SIMULATION AND DESIGN OF A 3-PHASE PWM AC-TO-DC RECTIFIER

A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of
Dokuz Eylül University
in Partial Fulfilment of the Requirements for
the Degree of Master of Science in Electrical and Electronics Engineering

by
Tolga SÜRGEVİL

December, 1997
İZMİR

M.Sc. THESIS EXAMINATION RESULT FORM

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Assoc.Prof.Dr. Eyüp AKPINAR

(Advisor)

.....

(Committee Member)

.....

(Committee Member)

Approved by the

Graduate School of Natural and Applied Sciences

Prof. Dr. Cahit HELVACI

Director

ACKNOWLEDGMENTS

I wish to express my gratitude to my advisor, Assoc. Prof. Dr. Eyüp AKPINAR, for his guidance and valuable suggestions during this study of thesis, and Mehmet VAR for his assistance during experimental measurements. I am indebted to my family for their support and patience.

Tolga SÜRGEVİL

ABSTRACT

A dedicated simulation program for a 3-phase pulse width modulated ac-to-dc rectifier under the predicted current control with fixed switching frequency (PCFF) and its implementation in the laboratory are presented in this thesis. This thesis gives the mathematical model of the rectifier and introduces the proposed control strategy. The dedicated simulation program uses this mathematical model and analyses overall system under the specified control logic. The line currents at the input of the rectifier are sinusoidal at unity power factor. The theoretical results of the simulation program containing steady-state and transient waveforms are experimentally verified.

ÖZET

Bu tezde sabit anahtarlama frekansında tahmini akım kontrolu (PCFF) yöntemi altında çalışan 3-faz darbe genişlik bindirimli ac-dc doğrultucu için yazılan benzetim programı ve laboratuvarda kurulan devre uygulaması tanıtılmaktadır. Doğrultucunun matematiksel modeli verilmekte ve uygulanacak kontrol stratejisi tanıtılmaktadır. Yazılan benzetim programı bu matematiksel modeli kullanarak tüm sistemin belirtilen kontrol mantığı altında çözümlemesini yapmaktadır. Devrenin uygulanmasında doğrultucu giriş akımlarının sinüs şeklinde ve giriş güç faktörünün bir olması hedeflenmiş ve gerçekleştirilmiştir. Sürekli hal ve geçici durum işaretlerini içeren benzetim programı sonuçları deneysel olarak elde edilenlerle karşılaştırılmaktadır.

CONTENTS

Page

Contents VII
List of Figures IX
List of Tables XI

Chapter One
INTRODUCTION

1. INTRODUCTION 1

Chapter Two
PULSE WIDTH MODULATED RECTIFIERS

2. PULSE WIDTH MODULATED RECTIFIERS 4
2.1 POWER FACTOR CONTROL IN PULSE WIDTH MODULATED RECTIFIERS 4
2.2 MATHEMATICAL MODEL OF A 3-PHASE PULSE WIDTH MODULATED RECTIFIER 10
2.3 PREDICTED CURRENT CONTROL WITH FIXED SWITCHING FREQUENCY 14

Chapter Three
SIMULATION PROGRAM

3.SIMULATION PROGRAM 19
3.1 PROGRAM ALGORITHM AND FLOW-CHART 19

3.2 RUNGE-KUTTA ALGORITHM..... 21
3.3 PI PARAMETER DESIGN..... 23

Chapter Four

IMPLEMENTATION OF PULSE WIDTH MODULATED RECTIFIER

4. IMPLEMENTATION OF PULSE WIDTH MODULATED RECTIFIER..... 25
4.1 RECTIFIER CIRCUIT..... 26
4.2 GATE DRIVE CIRCUIT..... 27
4.3 CONTROL CIRCUIT..... 28
4.4 AUXILIARY CIRCUITS..... 30
4.4.1 Snubber Circuits..... 30
4.4.2 Dead-Time Circuit..... 31
4.4.3 Current Sensors..... 33

Chapter Five

SIMULATION AND EXPERIMENTAL RESULTS

5. SIMULATION AND EXPERIMENTAL RESULTS..... 35

Chapter Six

CONCLUSIONS

6. CONCLUSIONS..... 45
REFERENCES..... 46
APPENDIX A..... 48
APPENDIX B..... 63

LIST OF FIGURES

		Page
Figure 2.1	The circuit of a 3-phase PWM ac-to-dc rectifier	5
Figure 2.2	Phasor diagrams for rectification and inversion modes at unity power factor	6
Figure 2.3	Control signals and switching waveforms for a 3-phase PWM rectifier	9
Figure 2.4	Phasor diagram for a desired leading power factor angle θ	9
Figure 2.5	The main circuit of a 3-phase PWM rectifier	10
Figure 2.6	Modelling of a 3-phase PWM rectifier circuit	11
Figure 2.7	Block scheme of a 3-phase PWM rectifier under PCFF	15
Figure 2.8	Waveforms of voltage/trigger converter	15
Figure 3.1	Flow-chart of the simulation program	20
Figure 3.2	Runge-Kutta method	23
Figure 3.3	Closed-loop transfer function of overall system	24
Figure 3.4	Root-locus of the open-loop transfer function of the system	24
Figure 4.1	The scheme of the implemented system	25
Figure 4.2	Pin-out and functional block diagram of IR2113	27
Figure 4.3	Gate drive circuit	28
Figure 4.4	Control circuit	29
Figure 4.5	RC protection circuit and optimal design curves	32
Figure 4.6	Dead-time circuit	33
Figure 4.7	Timing diagram of the dead-time circuit	34
Figure 4.8	LEM current sensor	34
Figure 5.1	Line-to-neutral voltage and line current of phase A (from simulation)	37

Figure 5.2 Line-to-neutral voltage and line current of phase A (from experiment)..... 37
Figure 5.3 DC output voltage (from simulation)..... 38
Figure 5.4 DC output voltage (from experiment)..... 38
Figure 5.5 Line-to-neutral and rectifier input voltage of phase A (from simulation)..... 39
Figure 5.6 Line-to-neutral and rectifier input voltage of phase A (from experiment). 39
Figure 5.7 Line-to-neutral and command voltage of phase A (from simulation)..... 40
Figure 5.8 Line-to-neutral and command voltage of phase A (from experiment). 40
Figure 5.9 Line current and command current of phase A (from simulation)..... 41
Figure 5.10 Line current and command current of phase A (from experiment)..... 41
Figure 5.11 Line current of all phases (from simulation). 42
Figure 5.12 Line current of all phases (from experiment)..... 42
Figure 5.13 Transient waveform of dc output voltage during the change of R_0 from 384 ohms to 192 ohms (from simulation)..... 43
Figure 5.14 Transient waveform of dc output voltage during the change of R_0 from 384 ohms to 192 ohms (from experiment)..... 43
Figure 5.15 Transient waveform of line current of phase A during the change of R_0 from 384 ohms to 192 ohms (from simulation)..... 44
Figure 5.16 Transient waveform of line current of phase A during the change of R_0 from 384 ohms to 192 ohms (from experiment)..... 44

LIST OF TABLES

Page

Table 3.1 Fourth-order Runge-Kutta method..... 22

Table 5.1 System parameters..... 35

CHAPTER ONE
INTRODUCTION

Low input power factor and high total harmonic distortion of input current of the diode or thyristor rectifiers are very important problem at high power ratings in industrial applications. Distorted line current waveforms of such kind of rectifiers with reactive loads, like many of ones used in industry, causes harmonic pollution in interconnected electric networks. Official regulations and constraints against harmonic distortion and low power factor prompted researchers to modify the design of rectifiers. In addition, incapability of regenerative operation are the restrictive factors in many applications, especially in variable-speed dc motor drive systems. To overcome this problem, naturally commutated phase-controlled rectifiers are extensively used in variable-speed applications, but the power factor and harmonics are still a problem. The performance of these rectifiers of the kind very much depends on the phase delay angle of the thyristors and the power factor of the load. Input filters to correct input power factor and to eliminate the harmonic contents of line currents are of large size with the growing amount of KVA and bring about extra costs. Moreover, dual converters allowing four-quadrant operation are not preferred in some applications because of their high cost and complexity of control circuit.

Considering the criteria mentioned above, pulse width modulated ac-to-dc rectifiers seem to give the best solution to these problems. With the spreading usage of high-power switching devices, such as IGBTs, power MOSFETs, and GTOs, PWM rectifiers are widely used in power conversion. The benefits of pulse width modulated rectifiers can be listed as follow;

1. Rectifier input current is almost sinusoidal, ie. low total harmonic distortion without needing any input filter.
2. Unity and leading input power factor adjustment, which provides reactive power compensation.
3. Regenerative capability, ie. allowing current flow from the load to the supply, which provides energy saving by returning the energy to the supply in motor drive applications.
4. Less circuit complexity in comparison with the circuits designed to meet the discussed requirements.

Up to now, many of control circuits for PWM rectifiers have been suggested in published papers. All of them try to accomplish the same duties listed above, but each circuit is different from the others with respect to its logic and performance. Phase-amplitude control (PAC), hysteresis current control (HCC), indirect current control (ICC), and predicted current control with fixed switching frequency (PCFF) are the several ones of them.

In hysteresis current control, line current error is aimed to be kept in a defined hysteresis band. It has a fast dynamic response and is easy to implement. However, average switching frequency increases with heavy loads, which results in stresses on switching devices (OOI, B.T., SALMON, J.C., DIXON, J.W., KULKARNI, A.B., 1987).

Indirect current control provides a standard sinusoidal PWM signal. The main advantage of this method is the elimination of the need to the current transducers. Stability region is restricted by parameter values in this method (DIXON, J.W., & OOI, B.T., 1988).

Predicted current control with fixed switching frequency depends on the prediction of the line current values from an error signal at the dc side. Speed and accuracy are the benefits of this method. However, it is parameter sensitive depending on the load variations (WU, R., DEWAN, S.B., & SLEMON, G.R., 1990)-(WU, R., DEWAN, S.B., & SLEMON, G.R., 1991, 27/4)

Phase-amplitude control is based on the control of the fundamental component of the rectifier input voltage with the modulation index and the phase delay of a sinusoidal control signal. It has a simple structure. Unity power factor is attained and the line current

harmonics are reduced. However, stability problems may occur at low load resistance (WU, R., DEWAN, S.B., & SLEMON, G.R., 1987)-(WU, R., DEWAN, S.B., & SLEMON, G.R., 1991, 27/2).

The purpose of this thesis is to simulate and design a 3-phase PWM ac-to-dc rectifier circuit under the predicted current control method, which is briefly discussed above, and to search the validity of the model by comparing the results with experimental ones. To achieve that, a dedicated simulation program has been written in FORTRAN programming language. Afterwards, an experimental set-up of the rectifier circuit has been built in the laboratory and the simulation results have been verified.

In Chapter II, the concept of power factor control in PWM rectifiers, and the proposed control strategy, predicted current control with fixed switching frequency, will be discussed together with the mathematical model of a 3-phase PWM rectifier.

The dedicated simulation program is introduced in Chapter III. Also, Runge-Kutta method used in the solution of differential equations and the design of PI parameters will be given.

Chapter IV gives the overall system that has been realised, and design criteria. The system will be introduced in stages of rectifier, gate driver, control, and other auxiliary circuits.

Finally, simulation and experimental results are presented in Chapter V, including steady-state and transient waveform

CHAPTER TWO

PULSE WIDTH MODULATED RECTIFIERS

Pulse width modulated (PWM) rectifiers have many advantages in comparison with the uncontrolled and phase-controlled rectifiers. The feature of operating as a converter, ie. they can operate as both rectifier and inverter, makes them superior to diode and thyristor rectifiers in respect of regenerative operating capability. Additionally, line currents are improved in PWM rectifiers, which means a very low harmonic distortion. And of most importance, these line currents are so controlled that unity or leading power factor can be achieved.

In this chapter, the logic of the power factor control in PWM rectifiers will be introduced. The mathematical model of a 3-phase PWM ac-to-dc rectifier and the control strategy to be applied to the rectifier circuit will be given in the following sections.

2.1 POWER FACTOR CONTROL IN 3-PHASE PWM RECTIFIERS

From the viewpoint of circuit theory, the power factor is defined as the cosine of the angle between the voltage and the current waveforms. In fact, this definition is valid for sinusoidal voltage and current waveforms. The most of the circuits in power electronics draw non-sinusoidal currents. The power factor is usually defined as follows for the non-sinusoidal currents;

$$\text{Power Factor} = \frac{I_{s1}}{I}\cos\phi \qquad (2.1)$$

where, cosϕ is the displacement factor, which is the cosine of the displacement angle (ϕ) between the supply voltage and the fundamental component of the supply current. I_{s1} is the rms value of the fundamental component of the input current and I_s refers to the rms value of the input current. The ratio I_{s1}/I_s can be defined as input distortion factor and gives an idea about how much the line currents are distorted. For sinusoidal line currents, the distortion factor is equal to one. From the equation (2.1), it is clear that in order to improve the power factor, the line currents must be also improved in shape as well as the displacement angle (LANDER, C.W. ,1993).

Figure 2.1 shows a 3-phase PWM ac-to-dc rectifier circuit. In this circuit, the power factor control logic depends on the control of the power flow from supply to the rectifier. If the power flow is controlled, the line currents are also controlled as a consequence. As a result of this, unity power factor can be achieved or leading power factor adjustment can be done.

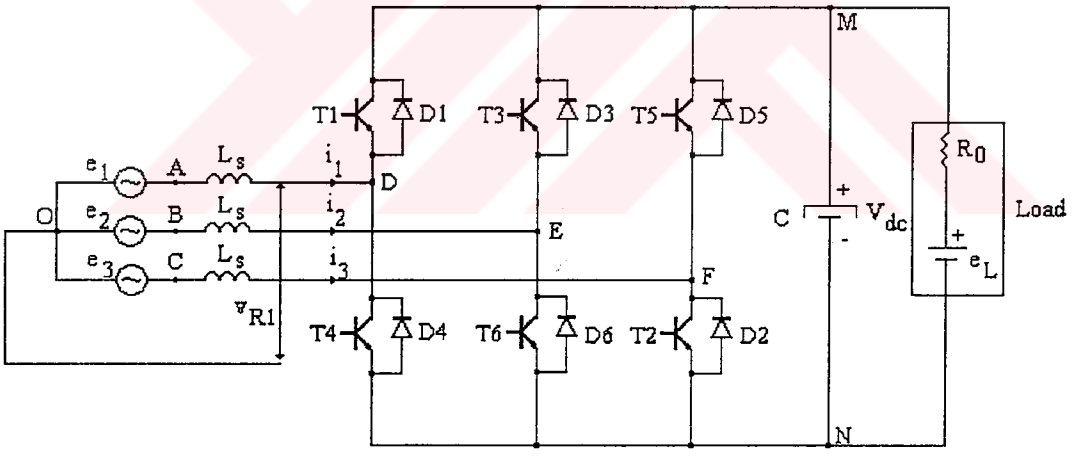


Figure 2.1 The circuit of a 3-phase PWM ac-to-dc rectifier

The instantaneous values of 3-phase supply voltages are;

$$e_1 = V_m \sin(\omega t), \quad e_2 = V_m \sin(\omega t - 120°), \quad e_3 = V_m \sin(\omega t + 120°) \qquad (2.2)$$

where,

$$\omega = 2\pi f_{supply} \tag{2.3}$$

and

$$V_1 = \frac{V_m}{\sqrt{2}} \tag{2.4}$$

is the rms value of the supply voltage of phase A. For a balanced circuit, the active power drawn from the supply per phase is;

$$P = V_1 I_1 \cos\theta \tag{2.5}$$

where I_1 is the rms value of the rectifier input current of phase A and θ is the phase delay between the infinite bus voltage and the line current. V_{R1} is the rms value of the line to neutral rectifier input voltage of phase A. We can express the voltage and current signals per phase in phasor diagrams as shown in Figure 2.2.

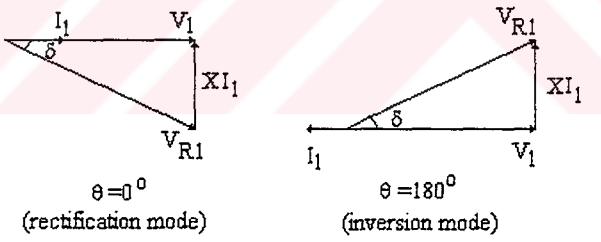


Figure 2.2 Phasor diagrams for rectification and inversion modes at unity power factor

The phasor diagrams describe the operation at unity power factor for rectification and inversion modes. Here, it is obvious that the rectifier input voltage should be greater then the ac supply voltage, which implies that the dc output voltage should also be greater than it. In the rectification mode, at which the real power flows from the infinite bus to the rectifier, V_1 leads V_{R1}. In the inversion mode, at which the real power flows from the rectifier to infinite bus, V_{R1} leads V_1. δ is the load angle and determines the departure of the fundamental component of the rectifier input voltage (V_{R1}) from the supply voltage (V_1). Using phasor relations;

$$\sin\delta = \frac{XI_1}{V_{R1}} \tag{2.6}$$

and

$$I_1 = \frac{V_{R1}}{X}\sin\delta \tag{2.7}$$

Substituting (2.7) into (2.5) for unity power factor, ie. cosθ=1;

$$P = \frac{V_1 V_{R1}}{X}\sin\delta \tag{2.8}$$

Here, X is the impedance of the source inductance in the ac line at the supply frequency and given by;

$$X = \omega L_s \tag{2.9}$$

As the equation (2.8) and the Figure 2.2 implies, the active power drawn from the supply can be controlled with the magnitude of the rectifier input voltage (V_{R1}) and the load angle (δ). The rectifier input voltage is controlled via switches reflecting the dc output voltage to the ac side. The switches are triggered by the comparators of which outputs give variable width pulses. To obtain switching signals, a sinusoidal control signal is compared with a triangular wave and at the intersection points the pulses are generated as shown in Figure 2.3. As mentioned before, the magnitude of the rectifier input voltage is controlled with a modulation index (M) and the load angle is controlled by the phase delay of the control signal (α). Here,

$$M = \frac{A_c}{A_w} \tag{2.10}$$

where A_c and A_w are the magnitudes of the control signals (v_{c1}, v_{c2}, v_{c3}) and the triangular wave, respectively. The rms value of the rectifier input voltage can be written as (WU, R., DEWAN, S.B., & SLEMON, G.R., 1987);

$$V_{R1} = KMV_{dc} \tag{2.11}$$

where, K is a fixed coefficient and V_{dc} is dc output voltage, which is at a desired constant value. The only way to change the magnitude of the rectifier input voltage is to change the modulation index according to (2.11). This is achieved by controlling the magnitude of the control signal. Additionally, the phase delay angle of the control signal determines the departure of the fundamental component of rectifier input voltage, ie. the load angle, as shown in Figure 2.3. Here, phase delay angle (α) is equal to load angle (δ), so the load angle control is attained by adjusting the phase delay angle of the control signal. In Figure 2.3, the instantaneous value of the rectifier input voltage has been obtained by using the following equation from Figure 2.5;

$$v_{R1}(t) = v_{DN}(t) + v_{NO}(t) \tag{2.12}$$

where,

$$v_{NO}(t) = -\frac{V_{dc}}{3}\sum_{k=1}^{3} d_k^{*} \tag{2.13}$$

which will be given in the following section in detail. The summation of the statues of T1, T3, and T5 gives Σd_k^*. The value of $v_{DN}(t)$ is either 0 or V_{dc} depending on the status of T1 and T4.

The rectifier can be operated at a desired power factor angle, too. Figure 2.4 shows phasor relations at a specified leading power factor angle. In that case, the active power is the one given in equation (2.8) and the reactive power is (MOHAN, N., UNDELAND, T.M. ,& ROBBINS, W.P., 1995);

$$Q = \frac{V_1^2}{X} - \frac{V_1 V_{R1}}{X}\cos\delta \qquad (2.14)$$

So, the power factor can be adjusted to unity or leading case obtaining appropriate rectifier input voltage and the load angle values and the power flow is controlled. This feature allows PWM rectifiers to be used also for reactive power compensation.

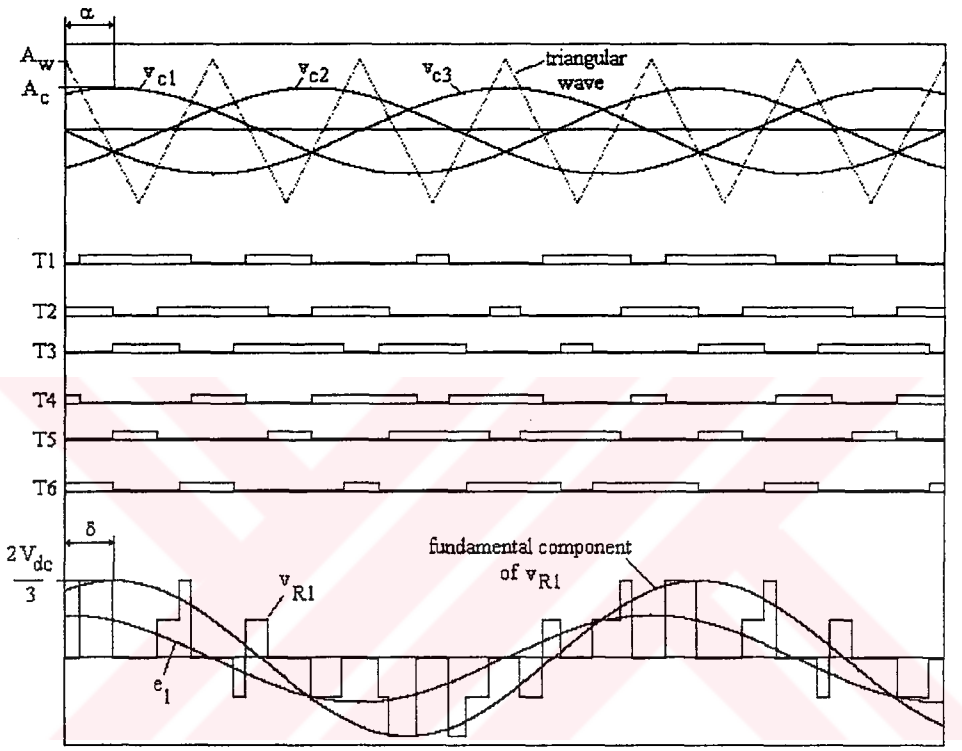


Figure 2.3 Control signals and switching waveforms for a 3-phase PWM rectifier

For rectification and inversion modes, the dc output voltage remains constant but the direction of the rectifier output current is reversed. This is the regenerative capability of PWM rectifiers and a very useful feature, especially in motor drive applications. For instance, during braking mode of a dc motor, a back electromotive force at the dc side exceeds dc output voltage and the energy can be delivered from the load to the supply by switching the transistors appropriately. In that case, the relevant rectifier input voltage and load angle values must be calculated by a control logic again.

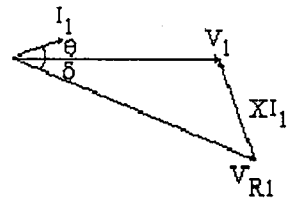


Figure 2.4 Phasor diagram for a desired leading power factor angle θ

2.2 MATHEMATICAL MODEL OF A 3-PHASE PWM RECTIFIER

The power stage of a 3-phase PWM ac-dc rectifier is given in Figure 2.5. The circuit consists of a balanced 3-phase supply voltages (e_1, e_2, e_3), boost inductances (L_s) at the ac side, six controlled semiconductor switching devices (T1-T6) such as IGBT, BJT, or MOSFET with anti-parallel diodes (D1-D6) in the rectifier part, the output capacitor (C), and a resistive load (R_0) with a back electromotive force (e_L) at the dc side.

The boost inductance takes its name from boost-type regulators, since the operation of this circuit similar to them. The dc output voltage is greater than the input voltage in boost-type regulators, so they are called with the name "boost". As mentioned in the previous section, the dc output voltage should be higher than the ac supply voltage at unity power factor in PWM rectifiers. Hence, the operation of these circuits are somewhat similar to boost regulators. The output capacitor must be selected at the value that it can hold its dc voltage at the constant value.

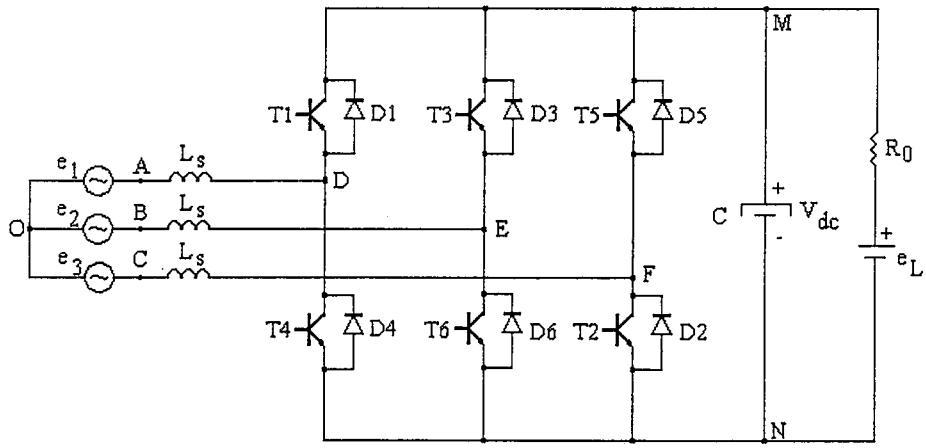


Figure 2.5 The main circuit of a 3-phase PWM rectifier.

Considering the switching devices as bilateral switches with a series resistance, which represents switching losses, and also taking the losses of the ac line into account, the circuit can be modelled as shown in Figure 2.6. As it can be seen clearly, R_L and R_s resistances are taken into the model in order to represent the losses of the circuit. Meanwhile, the load is assumed to be purely resistive in series to a constant dc voltage source e_L. Also, the inductances in the ac line are not supposed to have any magnetic saturation. The semiconductor devices of the same arm must not be turned on simultaneously in order to avoid a short-circuit of the dc output voltage (WU, R., DEWAN, S.B, SLEMON, G.R., 1990).

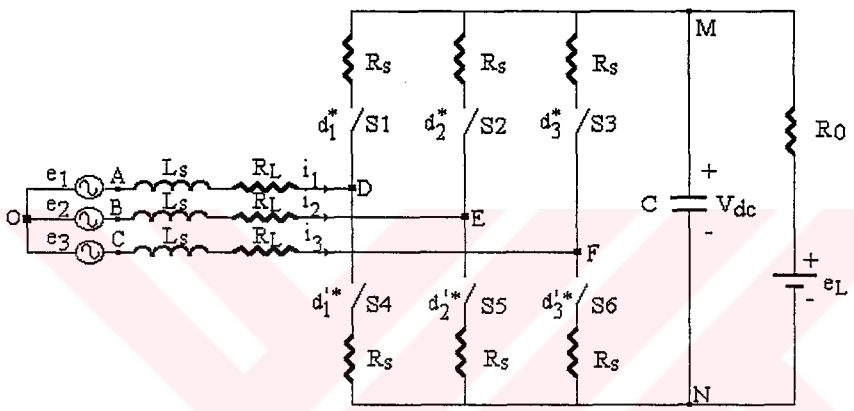


Figure 2.6 Modelling of a 3-phase PWM rectifier circuit

To obtain the equations of the circuit, Kirchoff's voltage law through each line and Kirchoff's current law at the terminal of positive dc voltage are held. The voltage equations for all phases are;

$$L_s\left(\frac{di_1}{dt}\right) + R_L i_1 = v_{AD} = e_1 - (v_{DN} + v_{NO}) \tag{2.15}$$

$$L_s\left(\frac{di_2}{dt}\right) + R_L i_2 = v_{BE} = e_2 - (v_{EN} + v_{NO}) \tag{2.16}$$

$$L_s\left(\frac{di_3}{dt}\right) + R_L i_3 = v_{CF} = e_3 - (v_{FN} + v_{NO}) \tag{2.17}$$

Here,

$$v_{DN} = \begin{cases} i_1 R_s + V_{dc} & \text{, when } d_1^* = 1 \;\; d_1'^* = 0 \\ i_1 R_s & \text{, when } d_1^* = 0 \;\; d_1'^* = 1 \end{cases} \tag{2.18}$$

$$v_{EN} = \begin{cases} i_2 R_s + V_{dc} & \text{, when } d_2^* = 1 \;\; d_2'^* = 0 \\ i_2 R_s & \text{, when } d_2^* = 0 \;\; d_2'^* = 1 \end{cases} \tag{2.19}$$

$$v_{FN} = \begin{cases} i_3 R_s + V_{dc} & \text{, when } d_3^* = 1 \;\; d_3'^* = 0 \\ i_3 R_s & \text{, when } d_3^* = 0 \;\; d_3'^* = 1 \end{cases} \tag{2.20}$$

And the differential equations are obtained as;

$$L_s(\frac{di_1}{dt}) + R_L i_1 = e_1 - \left[(i_1 R_s + V_{dc}) d_1^* + i_1 R_s d_1'^* v_{NO})\right] \tag{2.21}$$

$$L_s(\frac{di_2}{dt}) + R_L i_2 = e_2 - \left[(i_2 R_s + V_{dc}) d_2^* + i_2 R_s d_2'^* v_{NO})\right] \tag{2.22}$$

$$L_s(\frac{di_3}{dt}) + R_L i_3 = e_3 - \left[(i_3 R_s + V_{dc}) d_3^* + i_3 R_s d_3'^* v_{NO})\right] \tag{2.23}$$

since $d_k^* + d_k'^* = 1$ (k=1,2,3), equations can be simplified as;

$$L_s(\frac{di_1}{dt}) = e_1 - Ri_1 - (V_{dc} d_1^* + v_{NO}) \tag{2.24}$$

$$L_s(\frac{di_2}{dt}) = e_2 - Ri_2 - (V_{dc} d_2^* + v_{NO}) \tag{2.25}$$

$$L_s(\frac{di_3}{dt}) = e_3 - Ri_3 - (V_{dc} d_3^* + v_{NO}) \tag{2.26}$$

where $R = R_L + R_s$. Assuming that the 3-phase supply voltages are balanced;

$$e_1 + e_2 + e_3 = 0 \tag{2.27}$$

and since the system has no neutral line;

$$i_1 + i_2 + i_3 = 0 \tag{2.28}$$

$$\frac{di_1}{dt}+\frac{di_2}{dt}+\frac{di_3}{dt}=0 \tag{2.29}$$

v_{NO} can be obtained by the addition of the equations (2.24)-(2.26). Hence,

$$v_{NO}=-\frac{V_{dc}}{3}\sum_{k=1}^{3}d_k^* \tag{2.30}$$

Re-arranging the equations (2.24)-(2.26) with (2.30);

$$L_s(\frac{di_1}{dt})= e_1 - Ri_1 - (V_{dc}d_1^* - \frac{V_{dc}}{3}\sum d_k^*) \tag{2.31}$$

$$L_s(\frac{di_2}{dt})= e_2 - Ri_2 - (V_{dc}d_2^* - \frac{V_{dc}}{3}\sum d_k^*) \tag{2.32}$$

$$L_s(\frac{di_3}{dt})= e_3 - Ri_3 - (V_{dc}d_3^* - \frac{V_{dc}}{3}\sum d_k^*) \tag{2.33}$$

Finally, the node equation at the terminal M is;

$$C\frac{dv_{dc}}{dt}=i_1d_1^*+i_2d_2^*+i_3d_3^*-(\frac{v_{dc}-e_L}{R_0}) \tag{2.34}$$

So, the equations (2.24), (2.25), (2.26), and (2.34) give the state-space form of the model for the rectifier circuit. The compact form of the equations given above is as follows;

$$Z\dot{x}=A^*x+Be \tag{2.35}$$

where,

$$x=[i_1,i_2,i_3,v_{dc}]^T \tag{2.36}$$

$$e=[e_1,e_2,e_3,e_L]^T \tag{2.37}$$

$$A^* = \begin{bmatrix} -R & 0 & 0 & -(d_1^* - \frac{1}{3}\sum d_k^*) \\ 0 & -R & 0 & -(d_2^* - \frac{1}{3}\sum d_k^*) \\ 0 & 0 & -R & -(d_3^* - \frac{1}{3}\sum d_k^*) \\ d_1^* & d_2^* & d_3^* & \frac{-1}{R_0} \end{bmatrix} \quad (2.38)$$

$$Z = \begin{bmatrix} L_s & 0 & 0 & 0 \\ 0 & L_s & 0 & 0 \\ 0 & 0 & L_s & 0 \\ 0 & 0 & 0 & C \end{bmatrix} \quad (2.39)$$

$$B = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \frac{1}{R_0} \end{bmatrix} \quad (2.40)$$

Here, e is the input and x is the state matrices. The first order differential equation set is sufficient to describe the circuit with this model. The matrix A^*, which contains the switching duty ratios d_k^*, is time-variant because of the duty ratios' being a function of time. That means, it is quite difficult to obtain closed-form solutions. To overcome this difficulty, numerical integration methods are used for solving these differential equations, such as Runge-Kutta algorithm. In Chapter III, the simulation program is given, which aims to complete this task.

2.3 PREDICTED CURRENT CONTROL WITH FIXED SWITCHING FREQUENCY

This control method depends upon the prediction of the line current values from an error signal at dc side. The block scheme of a 3-phase PWM rectifier under the predicted current control with fixed switching frequency (PCFF) is given in Figure 2.7. Here, the difference between the reference dc voltage and the dc output voltage, ie. error signal, is converted to a magnitude information which is denoted as i_{cm}. This is the value to which the line currents are required to reach at the end of switching period. If it is done so, line currents

can be controlled with a reference current template, so unity or leading power factor can be achieved with almost sinusoidal line currents. To achieve unity power factor, i_{cm} signal is modulated with reference sinusoidal signals which are obtained from utility voltages. Thus, the reference current waveforms, named i_{ck}, are handled and the line currents are forced to follow this template waveforms by transforming these signals into appropriate control signals, named v_{ck}. Afterwards, this control signals, here called command voltages, are compared with a triangular waveform and the switching functions, d_k*, are obtained.

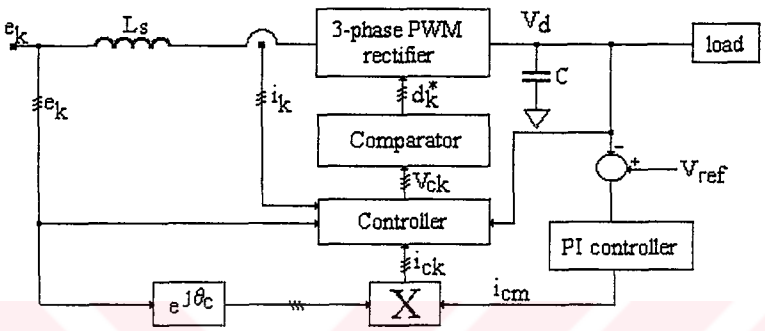


Figure 2.7 Block scheme of a 3-phase PWM rectifier under PCFF

If the switching period (T_s) is much higher than the frequency range of the command voltages, these can be treated as dc within one switching period and the average value of the switching functions (d_k) can be replaced with the switching functions as shown in Figure 2.8.

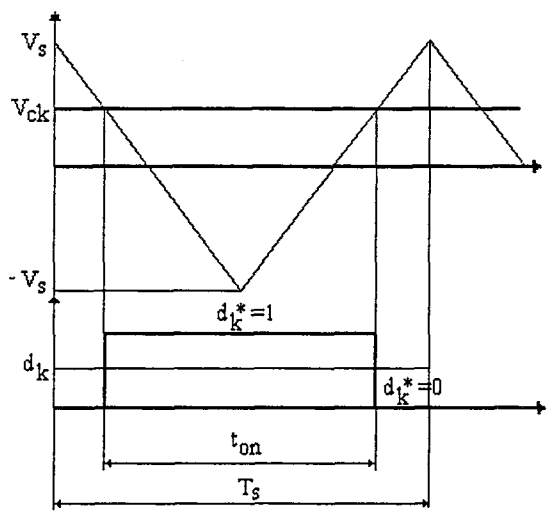


Figure 2.8 Waveforms of voltage/trigger converter

As mentioned above, the logic of the method is to force the line currents from their present values to the predicted values, which are determined as command currents. In that case, the rate of the change of the line currents should be as given in (2.41) within one switching period;

$$\frac{di_k}{dt} = \frac{i_{ck} - i_k}{T_s} \tag{2.41}$$

and

$$i_{ck} = i_k + T_s \frac{di_k}{dt} \tag{2.42}$$

From this equation, it is obvious that the line currents will follow the command currents with a switching delay of T_s. Since the sinusoidal line current are required, i_{ck} should have the form;

$$i_{ck} = i_{cm} \cos\left[\omega t + \theta_c - (k-1)\frac{2\pi}{3}\right] \tag{2.43}$$

where θ_c is the adjustable phase angle.

The state equations given in (2.31)-(2.33) will become as follow letting $d_k^* = d_k$;

$$L_s\left(\frac{i_{ck} - i_k}{T_s}\right) = \left[e_k - Ri_k - (V_{dc} d_k + v_{NO})\right] \tag{2.44}$$

then,

$$d_k = \frac{1}{V_{dc}}\left[e_k - (R - \frac{L_s}{T_s}) - \frac{L_s}{T_s} i_{ck}\right] - \frac{1}{V_{dc}} v_{NO} \tag{2.45}$$

putting (2.30) into (2.45),

$$d_k = \frac{1}{V_{dc}}\left[e_k - (R - \frac{L_s}{T_s}) - \frac{L_s}{T_s} i_{ck}\right] - \frac{1}{V_{dc}}(-\frac{V_{dc}}{3}\sum_{k=1}^{3} d_k) \tag{2.46}$$

hence,

$$d_k = \frac{1}{V_{dc}}\left[e_k - (R - \frac{L_s}{T_s}) - \frac{L_s}{T_s} i_{ck}\right] + \frac{1}{3}\sum_{k=1}^{3} d_k) \tag{2.47}$$

Here, it is assumed that (WU, R., DEWAN, S.B., SLEMON, G.R., 1990);

$$\sum_{k=1}^{3} d_k = \frac{3}{2} \tag{2.48}$$

so, (2.47) becomes,

$$d_k = \frac{1}{V_{dc}}\left[e_k - (R - \frac{L_s}{T_s}) - \frac{L_s}{T_s} i_{ck}\right] + \frac{1}{2} \tag{2.49}$$

Reference current waveforms (or command currents) are not meaningful alone. They just form a step in the generation of the switching signals. As shown in Figure 2.8, these command currents are converted to the command voltages, v_{ck}, and comparing those voltages with a triangular waveform, switching signals are generated for each arm of the rectifier circuit. The equation for the command voltages is obtained as follows;

$$d_k = \frac{t_{on}}{T_s} = \frac{v_{ck}}{2V_s} + \frac{1}{2} \tag{2.50}$$

substituting (2.50) into (2.49),

$$v_{ck} = \frac{2V_s}{V_d}\left[e_k - (R - \frac{L_s}{T_s})i_k - \frac{L_s}{T_s} i_{ck}\right] \tag{2.51}$$

Thus, the logic to obtain the switching functions is established. One can see that the rectifier input voltages are controlled with the command voltages. That means, the fundamental component of rectifier input voltages should be in the same shape as the command voltages. So, the modulation index and the load angle of the control signal mentioned in Section 2.1, here the command voltages, are obtained indirectly.

As shown in Figure 2.7, the supply voltages, which modulate the command current, is time delayed with θ_c. This time delay is provided in order to compensate switching delays as mentioned in equation (2.42) and obtained from the steady-state calculations. It can be calculated as follows (WU, R., DEWAN, S.B., SLEMON, G.R., 1991, 27, pp 757-761);

$$\theta_c = \tan^{-1}(\Omega T_s) \tag{2.52}$$

where,

$$\Omega = 2\pi f_{supply} \tag{2.53}$$

This method is used as the control logic of the rectifier circuit in this thesis because of its being easy to implement. The simulation program and the system has been designed depending upon this method. These will be introduced in Chapter III and Chapter IV, respectively.

CHAPTER THREE
SIMULATION PROGRAM

In this chapter, the dedicated simulation program for a 3-phase PWM rectifier under the predicted current control with fixed switching frequency (PCFF) will be introduced. The mathematical model of a 3-phase PWM converter has been given in Chapter II and the proposed control strategy has also been introduced. Considering both mathematical model and control logic, the simulation program, which refers to the system given in Figure 2.7 in Chapter II, has been written. FORTRAN programming language was used in this program with FORTAN 5.1 Compiler. The outputs of the program were stored in data files and using the graphics libraries of the compiler, graphical illustrations were obtained. These will be presented in Chapter V. The list of the programs are given in Appendix A.

3.1 PROGRAM ALGORITHM AND FLOW-CHART

The flow-chart of the simulation program is given in Figure 3.1. At the first stage, an error signal is obtained subtracting the current value of dc output voltage (V_{dc}) from the reference voltage (V_{ref}). Since PCFF method is based on the prediction of line current values from an error signal, this error signal should be converted to the magnitude of command currents denoted as i_{cm}. This is achieved by means of a PI controller. The output of the proportional controller is simply the multiplication of error signal with proportional gain (K_P). In order to obtain the output of the integral controller, the following equations are written;

$$x_I = K_I \int err(t)dt \qquad (3.1)$$

where, x_I is the output of integral controller and K_I is the integral gain.

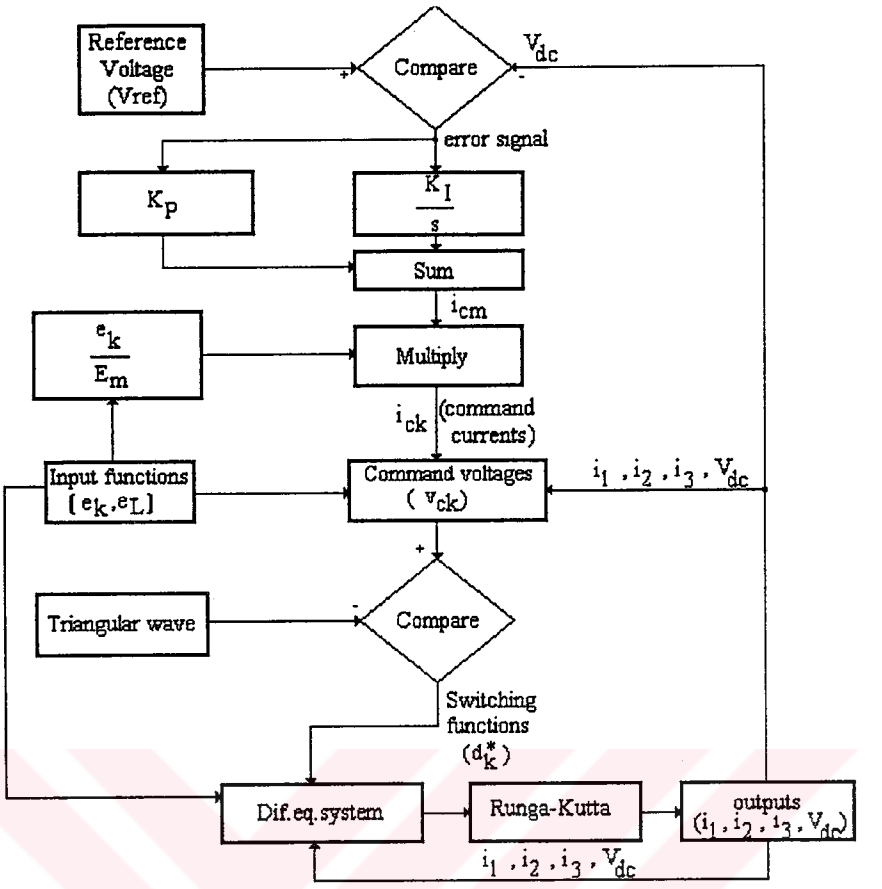


Figure 3.1 Flow-Chart of the simulation program

Re-arranging equation (3.1);

$$\frac{dx_I}{dt} = K_I err(t) \tag{3.2}$$

is obtained. The output of integral controller is calculated solving this differential equation with fourth-order Runge-Kutta algorithm. So, the output of PI controller is the summation of two individual controllers.

At the second stage, command currents (i_{ck}) are derived from the PI controller output (also the magnitude of command currents) and line voltages (e_k) for each phase. And then, command voltages (v_{ck}) are calculated using the mathematical expression, Equation (2.51) given in Chapter II.

At the third stage, switching functions (d_k*) are obtained comparing command voltages with a generated triangular waveform.

At the final stage, the differential equation system, Equation (2.31)-(2.34) in Chapter II, is solved using four-step Runge-Kutta algorithm, which will be introduced in the next section, and the outputs are handled from the inputs (e_1, e_2, e_3, e_L), switching functions, and the previous values of the outputs (i_1, i_2, i_3, V_d). This process is repeated up to 0.4 seconds of simulation time.

While using Runga-Kutta algorithm, step size for the iteration was chosen as $1x10^{-5}$ seconds, which was sufficiently small in comparison with the sampling period (T_s) of $0.32x10^{-3}$ seconds.

As mentioned earlier, outputs are stored in data files and are to be drawn using a graphical editor. This was achieved by an additional program using graphics libraries of FORTRAN 5.1 Compiler. So that, desired waveforms are monitored by making use of this program. The source codes of the simulation and graphics programs are given in Appendix A.

3.2 RUNGE-KUTTA ALGORITHM

Numerical methods are used in the solution of differential equations which cannot be solved in closed-form and are also applied to the equations of which solution is very complicated in such form. As can be seen from the mathematical model of the rectifier circuit in Chapter II, the equations are difficult to solve in closed-form since they are time variant. To avoid this difficulty, the equations were solved numerically applying the fourt-order Runge-Kutta algorithm.

Runge-Kutta algorithm is applied to the initial value problems of the first-order differential equations which is in the form;

$$y' = f(x, y) \qquad , y(x_0) = y_0 \tag{3.3}$$

where x_0 and y_0 are initial values.

Let the initial value of the function (y) be y_n at the point x_n. The struggle of this method is to calculate the value of y at the next step, ie. $y_1=y(x_1)=y(x_0+h)$, where h is the step size as shown in Figure 3.2. To achieve that, four quantities k_1,k_2,k_3,k_4 are computed first and then the y_{n+1} value at the point x_{n+1} is obtained following the procedure below (KREYSZIG, E. ,1993, pp. 1040-1041);

ALGORITHM RUNGE-KUTTA (f,x_0,y_0,h,N)

Input: Initial values x_0,y_0, step size h, number of step N

Output: Approximation y_{n+1} to the solution $y(x_{n+1})$ at $x_{n+1}=x_0+(n+1)h$, where n=0,1,...(N-1)

for n=0,1,...(N-1) do:

$$k_1 = hf(x_n, y_n)$$

$$k_2 = hf(x_n + \frac{h}{2}, y_n + \frac{k_1}{2})$$

$$k_3 = hf(x_n + \frac{h}{2}, y_n + \frac{k_2}{2})$$

$$k_4 = hf(x_n + h, y_n + k_3)$$

$$x_{n+1} = x_n + h$$

$$y_{n+1} = y_n + \frac{1}{6}(k_1 + 2k_2 + 2k_3 + k_4)$$

End

Stop

END RUNGE-KUTTA

Table3.1 Fourth-Order Runge-Kutta Method

This procedure is repeated as much as it is desired. The previous outputs are used at each time step as the initial values and the computation goes on in the same way.

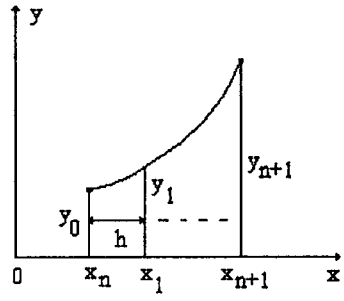


Figure 3.2 Runge-Kutta method

3.3 PI PARAMETER DESIGN

To estimate the proportional (K_P) and integral gain (K_I) parameters, the transfer function between the magnitude of the command currents (i_{cm}) and the dc output voltage (v_{dc}) is needed. This transfer function is obtained from the small signal model of the rectifier and given as (WU, R., DEWAN, S.B., SLEMON, G.R., 1991, 27, pp. 760-762);

$$G(s) = \frac{v_{dc}(s)}{i_{cm}(s)} = K_{vi} \frac{(1 - s/\omega_0)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{3.4}$$

where,

$$K_{vi} = \frac{3}{2} \frac{(E_m - 2I_{cm}R)}{V_{dc}(\frac{2 - E_L/V_{dc}}{R_0})} \tag{3.5}$$

$$\omega_0 = \frac{E_m - 2I_{cm}R}{LI_{cm}} \tag{3.6}$$

$$\omega_{p1} = \frac{2 - E_L/V_{dc}}{R_0 C} \tag{3.7}$$

$$\omega_{p2} = \frac{1}{T_s} \tag{3.8}$$

where, E_m is the peak value of the supply voltage, I_{cm} is the peak value of the command currents. Considering the system with a negative unity feedback as shown in Figure 3.3, appropriate PI parameters can be obtained from the root-locus of the open-loop transfer function of the system, ie. PI(s)G(s).

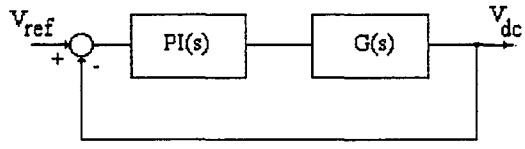


Figure 3.3 Closed-loop transfer function of overall system

The transfer function of the PI controller is;

$$PI(s) = K_P + \frac{K_I}{s} = K_P(1 + \frac{K_I / K_P}{s}) \qquad (3.9)$$

The root-locus of the open-loop transfer function depending on K_P is shown Figure 3.4. From this scheme, the closed-loop operation of the system is observed using Program CC. Here, K_P is chosen 1 with K_I/K_P=55.6 and the closed-loop poles are marked on the root-locus for the given parameter values.

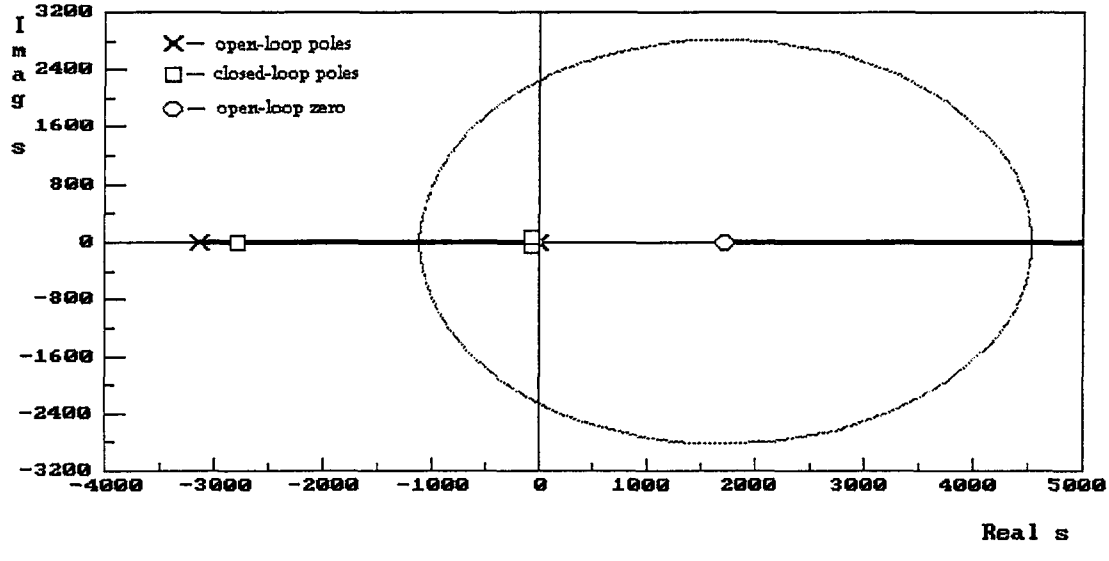


Figure 3.4 Root-locus of the open-loop transfer function of the system

CHAPTER FOUR

IMPLEMENTATION OF PULSE WIDTH MODULATED RECTIFIER

As a part of this thesis, a 3-phase PWM ac-to-dc rectifier circuit has been designed and implemented in Electrical Machines and Power Electronics laboratory. Predicted current control method introduced in Chapter II has been applied in the control of the circuit. The system parameters have been chosen the same as those given in Chapter III to make a comparison between the theoretical and experimental results, which are given in Chapter V.

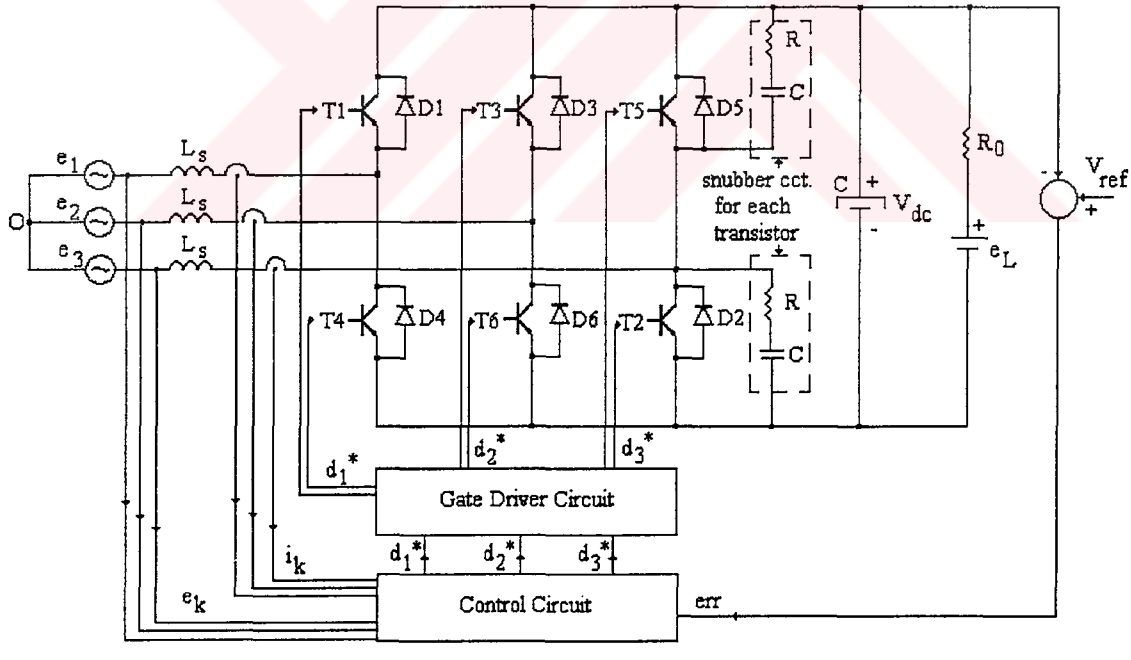


Figure 4.1 The scheme of the implemented system

The circuit has been implemented in two steps. First, it was operated without a dc output voltage feedback. In that case, the circuit that obtains the error signal and PI controller part

are missing in the control circuit given in Figure 4.4. A magnitude information is entered as a desired line current magnitude and these are modulated with the supply voltages. The control circuit parameters were set to the appropriate values depending on the operation point, which is determined by the system parameters given in Chapter III. It was observed that the line currents followed the command currents. But, during load changes, the dc output voltage value deviated from the operation point because the circuit tends to satisfy the following power equality;

$$3V_1I_1\cos\theta = \frac{V_{dc}^2}{R_0} \qquad (4.1)$$

where, V_1 and I_1 are the rms values of the phase A voltage and current, respectively. Here, $\cos\theta$ is the power factor and it was obtained at unity value. One can see that the line currents are forced to be kept at a steady value for the unity value of the input power factor from the equation (4.1). So, the ac power drawn from the supply should be constant. When the load changes, the output dc voltage should be adjusted to its new value by the system such that the output power remains constant according to (4.1). In order to keep the rectifier output voltage constant, the differentiator and the PI controller unit added to the system and the closed-loop operation is obtained at the second step.

The overall system in Figure 4.1 can be divided into four blocks. They are;

1. Rectifier Circuit
2. Gate Driver Circuit
3. Control Circuit
4. Auxiliary Circuits

4.1 RECTIFIER CIRCUIT

The main circuit of a 3-phase PWM rectifier has been given in Figure 2.2.1, in Chapter II. IRGPH30MD2 insulated gate bipolar transistors (IGBT) have been used as switching devices. These transistors are provided with anti-parallel protection diodes between collector and emitter, so there is no need to connect extra power diodes to the circuit. The

ratings, electrical characteristics, and switching characteristics of IRGPH30MD2 are given in Appendix B.

4.2 GATE DRIVE CIRCUIT

To drive a pair of transistors connected as a bridge leg has some difficulties. Especially, when driving an upper side transistor, the emitter voltage of the transistor takes the value of dc line voltage. In that case, the gate voltage of the transistor must be boosted up to dc line voltage plus transistor ON voltage with respect to the circuit ground to maintain the ON state. Here, IR2113 high and low side gate driver integrated circuits have been chosen because of their dedicated design for this task. The pin-out and functional block diagram of IR2113 is given in Figure 4.2. It is possible to drive a pair of IGBTs or MOSFETs with only one IR2113. There is no need to connect an extra interface to the circuit. In Figure 4.3, the gate drive circuit of one phase is given. The same circuit has been used for the other arms of the related phases. The other specifications of IR2113 are given in Appendix B.

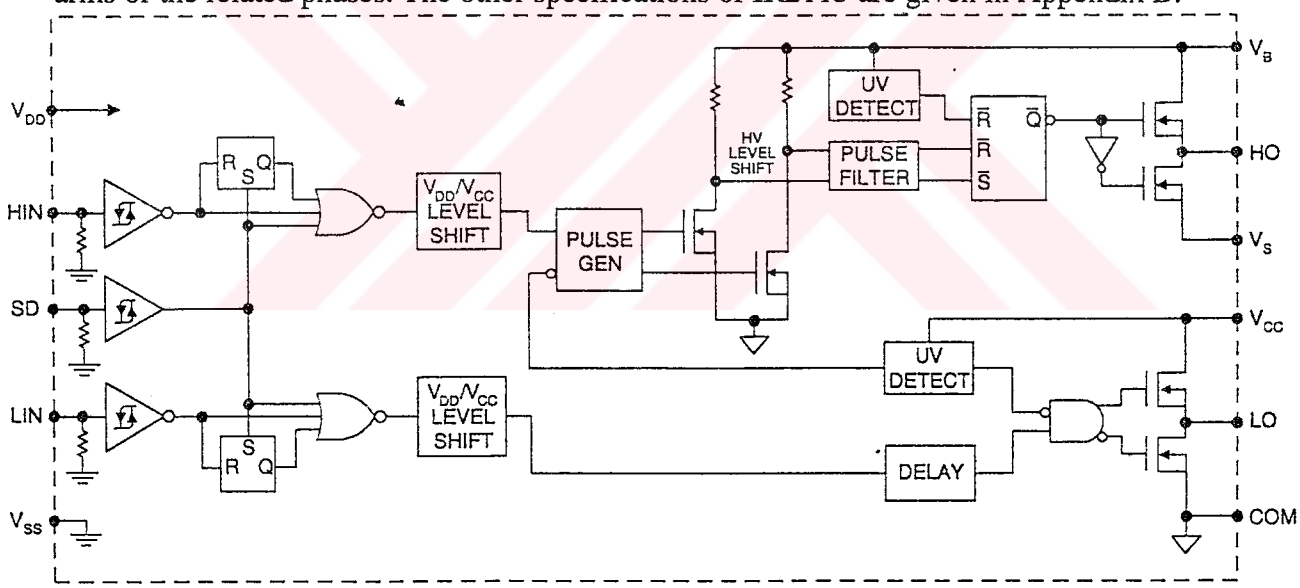


Figure 4.2 Pin-out and functional block diagram of IR2113

The gate signal of each transistor is connected to the input pins numbered 10 and 12 of the IC, HIN and LIN, respectively. For the lower side transistor, LO output switching waveform is the same as that of LIN, which is low side input switching waveform, with only a very little time delay specified in data sheets. For the upper side transistor, the bootstrap capacitor between the terminals 5 and 6, Vb and Vs, is charged up-to Vcc voltage quickly after an ON state of the lower side switch. When a signal incomes to HIN to hold

the upper side switch ON (in that case, the lower side switch must be OFF), Vs voltage is equal to dc line voltage with respect to the ground of the circuit and Vb voltage is boosted to the dc line voltage plus Vcc, since the bootstrap capacitor cannot discharge because of the diode across the terminals Vb and Vcc. So, as it can be seen from the functional block diagram of the IC, the MOSFETs at the output stage are kept ON and HO signal is now at the value of dc line voltage plus HIN voltage with respect to the circuit ground. Consequently, the ON signal of the upper side transistor is maintained.

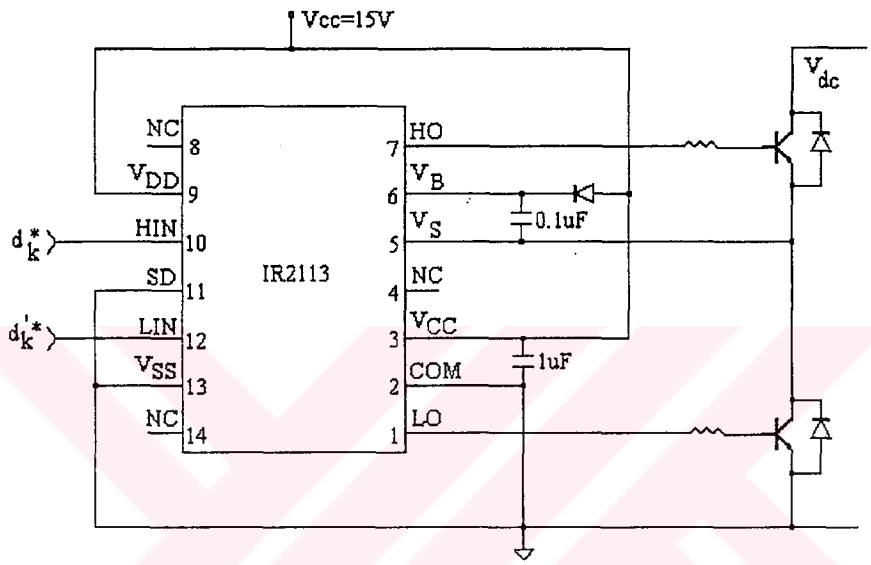


Figure 4.3 Gate Drive Circuit

4.3 CONTROL CIRCUIT

The control circuit is the most important part of the system. As mentioned before, the control circuit generates the command voltages (v_{ck}) and these voltages are then converted to the switching waveforms. The complete configuration of the control circuit is given Figure 4.4. It is completely designed in analog form.

In this circuit, the dc output voltage, which is attenuated by the ratio of 15/220, is compared with the dc reference voltage and the error signal is obtained first. This is achieved by a summing circuit with dc feedback and inverted dc reference voltage inputs.

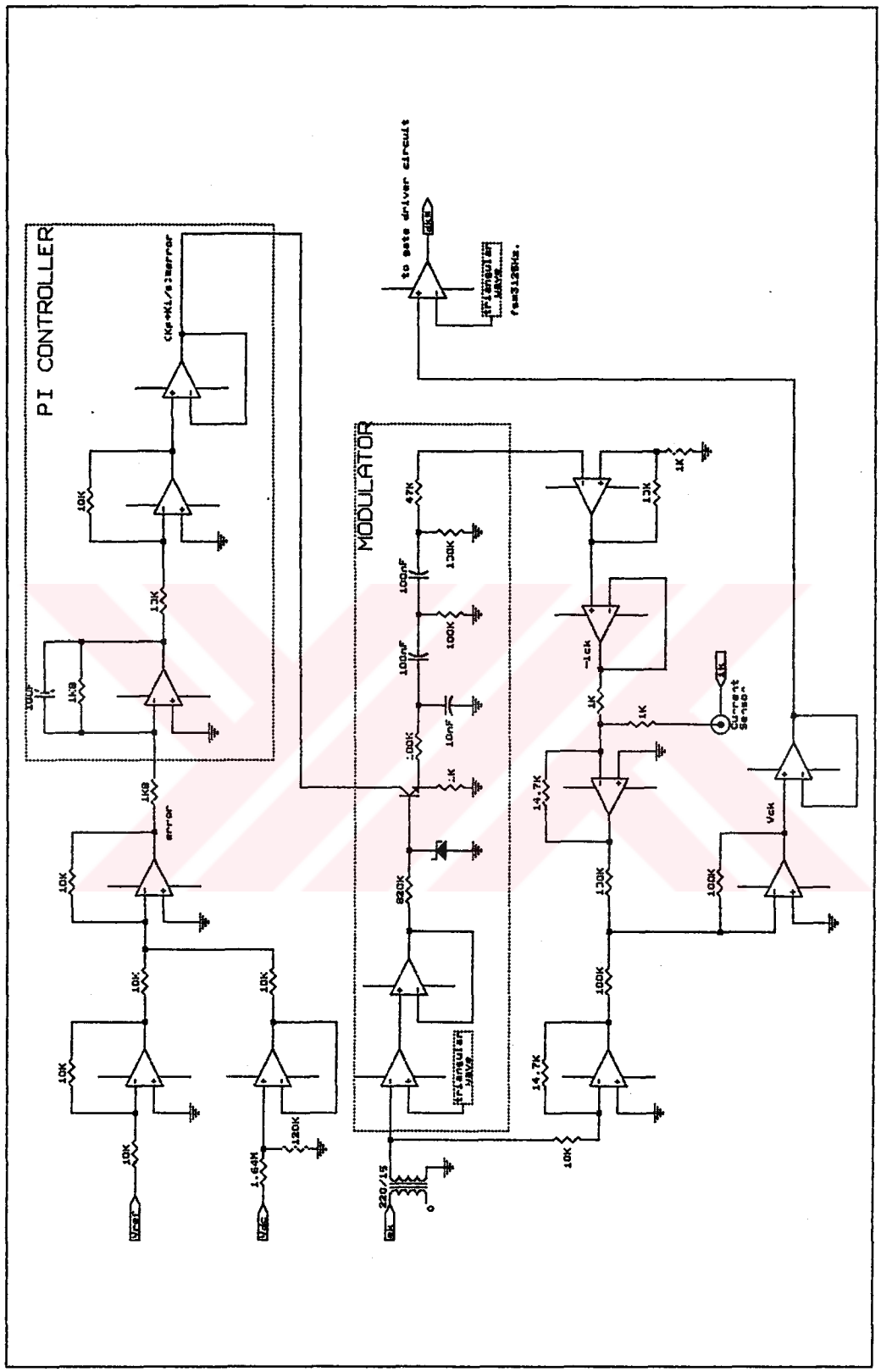


Figure 4.4 Control Circuit

This error signal is then passed through a PI type controller, which is shown in dashed lines. The proportional and the integral gain of this circuit can be calculated as follow;

$$\frac{err(t)-0}{R_i}+\frac{V_0(t)}{Z_{RC}}=0 \tag{4.2}$$

where Z_{RC} is the impedance of parallel RC circuit and;

$$Z_{RC}=R+\frac{1}{sC} \tag{4.3}$$

Then equation (4.2) becomes;

$$\frac{V_0(t)}{err(t)}=-(\frac{R}{R_i}+\frac{1}{sR_iC}) \tag{4.4}$$

The transfer function of a PI type controller has been given in Chapter III. So, the proportional and integral gains (K_P and K_I, respectively) of the circuit are;

$$K_P=\frac{R}{R_i} \tag{4.5}$$

and

$$K_I=\frac{1}{R_iC} \tag{4.6}$$

For the values of the components in the circuit, K_P=1 and K_I=55.6.

The output of the PI controller determines the magnitude of the command currents (i_{cm}). The i_{cm} signal is then modulated with the reference line voltages waveforms and the command currents of each phase are (i_{ck}) generated. Here it must be notified that the turns ratio of the voltage transformers, from which the reference line voltage shapes are taken, is

220/15, too. The modulator circuit is also indicated in dashed lines and its modulation technique depends on the PWM as it can be seen in Figure 4.4.

The rest of the circuit calculates the command voltages (v_{ck}), which has been given in equation (2.3.51), from the combination of e_k, i_k, and i_{ck}. Here, the gains of the circuit at the output stage, which is simply a summing amplifier, must be adjusted to an appropriate value so that the command voltages are produced properly. The circuit parameters are the same as those given in Chapter III. At the final stage, these command voltages are compared with a triangular waveform and the switching pulses are generated.

4.4 AUXILIARY CIRCUITS

The auxiliary circuits used in this system are the snubber circuits, the dead-time circuit, and the current sensors.

4.4.1 Snubber Circuits

An RC type snubber circuit has been designed for dV/dt protection of the IGBTs. The main object of the snubber circuit is to absorb the energy of the stray inductances, which may cause to high voltage drops on the transistors during turn-off and damage them. In Figure 4.5, the condition of any transistor during turn-off is given. Depending on the operating conditions of the circuit, damping and overshoot factors of the snubber circuit are also given in Figure 4.5. Assuming the stray inductance at a reasonable value of 100nH, the following calculations are made under the given operating conditions (WILLIAMS, B.W., 1992).

V_s=200V (dc line voltage), I_l=10A (line current), and f_s=3kHz. (switching frequency). For 20% overshoot, ζ=1.05, and χ=0.52. And,

$$C = L_{stray}\left(\frac{I_l}{\chi V_s}\right)^2 = 100\text{x}10^{-9}\left(\frac{10}{0.52\text{x}200}\right)^2 = 0.93\text{nF} \qquad (4.7)$$

$$R = 2\zeta\left(\frac{V_s\chi}{I_l}\right) = 2\text{x}1.05\left(\frac{200\text{x}0.52}{10}\right) = 21.84\text{ohms} \qquad (4.8)$$

So, the available values of C=1nF and R=18 ohms are chosen. The power ratings of the capacitor and resistor are;

$$W_{co} = \frac{1}{2} C V_s^2 f_s = \frac{1}{2} x1x10^{-9} x200^2 x3x10^3 = 0.06W \tag{4.9}$$

$$W_R = \frac{\tau}{t_{on} + \tau} W_{co} + \frac{\tau}{\tau + t_{off}} (W_{CO} + \frac{1}{2} L_{stray} I_1^2 f_s)$$
$$= \frac{2x18}{118} x0.06 + \frac{18}{118} x \frac{1}{2} x20x10^{-9} x10^2 x3x10^3 = 0.01W \tag{4.10}$$

where, τ=RC is the time constant of the snubber circuit and t_{on}=t_{off}, which are the rise and fall time of the transistor, were assumed to be 100ns. Power ratings of the components were chosen according to these values.

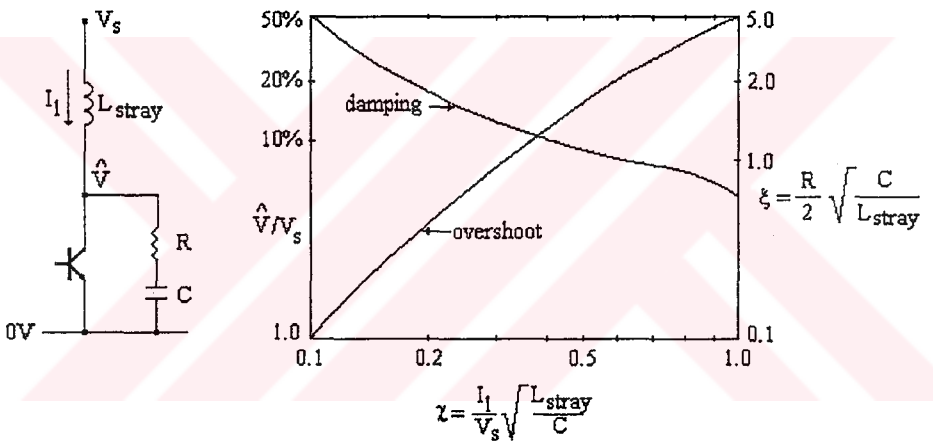


Figure 4.5 RC protection circuit and optimal design curves

4.4.2 Dead-Time Circuit

The dead-time circuit can be seen in Figure 4.6. The purpose of this circuit is to prevent a short circuit condition of the dc output voltage because of the rising and fall time of the transistors in the same leg (PRAVADALIOĞLU, S., 1995).

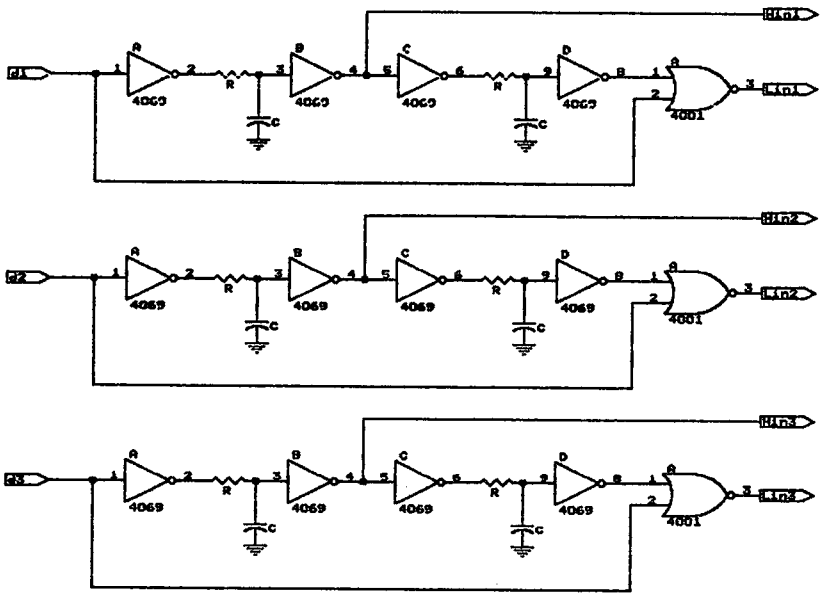


Figure 4.6 Dead-time Circuit

To prevent the short circuit, time delay as much as the rising or fall time of the transistor is necessary while changing the positions of the transistors. This is achieved by this circuit. In Figure 4.7, the timing diagram of the circuit is given. The dead-time period is calculated from the following formula;

$$V_c(t) = V_{cc}\left[1 - \exp(-t_d / \tau)\right] \tag{4.11}$$

where $V_c(t)$ is the capacitor voltage ,V_{cc} is the supply voltage, and τ is the time constant of the RC circuit. For Vcc=15V and 20 percent zero threshold level;

$$3 = 15x\left[1 - \exp(-t_d / \tau)\right] \tag{4.12}$$

and

$$t_d = 0.097\tau = 0.097RC \tag{4.13}$$

For the given values of the components (R=4K7 and C=1nF), time delay is 0.46 microseconds for this circuit.

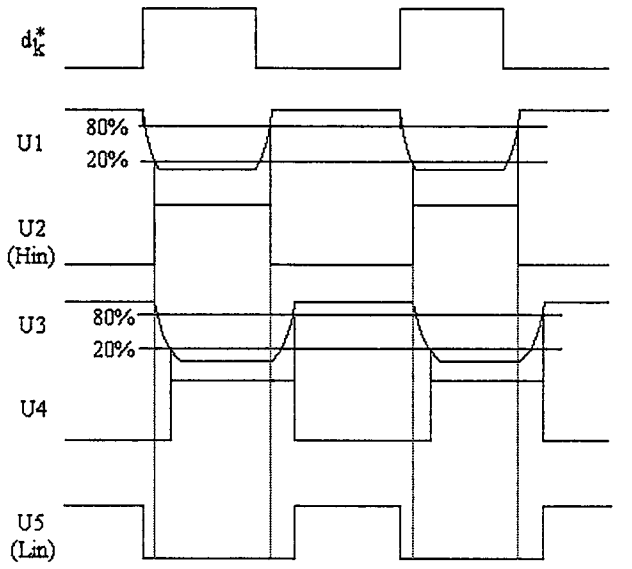


Figure 4.7 Timing diagram of the dead-time circuit

4.4.3 Current Transducers

To obtain the line current values, LEM Hall-Effect Current Modules are used in this system. The advantage of using these sensors is the facility of isolation from the power circuit. As shown in Figure 4.8, the line current to be measured is passed through the measurement hall provided on the module. These modules require a +-15V supply and the current measurement is taken from across the resistor connected between the point M of the transducer and the ground of the supply as shown in Figure 4.8. The value of the resistor is adjusted so that it gives 1V output at 1A current value.

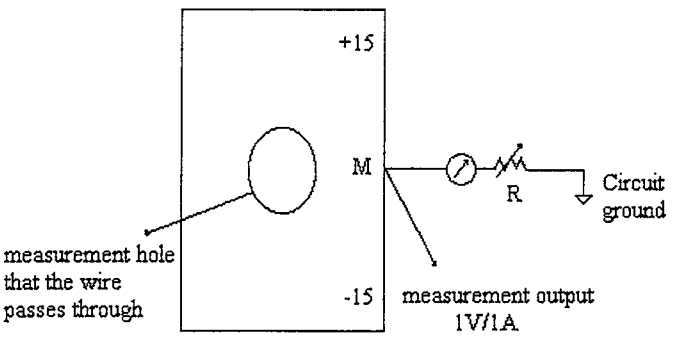


Figure 4.8 LEM Current Sensor

CHAPTER FIVE
SIMULATION AND EXPERIMENTAL RESULTS

In this chapter, the simulation and the experimental results of the implemented rectifier circuit will be presented. These results includes both steady-state waveforms, which were obtained at a load resistance value of 384 ohms, and transient waveforms, which were obtained during a load change from 384 ohms to 192 ohms. It is observed that the experimental results are very close to theoretical ones. Considering the block diagram given in Figure 2.7 in Chapter II, the parameters of the system were chosen as shown in Table 5.1;

Parameter	Symbol	Value
3-phase supply voltages	e_k	$60\cos(2\pi 50t-(k-1)*2\pi/3)$
Boost inductance per phase	L_s	45mH
total ac resistance per phase	R	2.4Ω
dc side capacitor	C	4.5mF
back emf of the load	e_L	0V
dc load resistance	R_0	384Ω
sampling period	T_s	0.32ms
dc reference voltage	V_{ref}	165V
phase delay to compensate the switching delays	θ_c $(\tan^{-1}\omega T_s)$	5.74^o
PI controller gains	K_P, K_I	1, 118

Table 5.1 System parameters

In Figure 5.1 and 5.2, the waveforms of line-to-neutral source voltage and line current of phase A are given, which are obtained from simulation and experiment, respectively. The line current waveform is almost sinusoidal and unity power factor is achieved.

Figure 5.3 and 5.4 show the dc output voltage from simulation and experimental work, respectively. It is almost held at a constant value and contains very low ripple content.

Figure 5.5 and 5.6 show the relation between line-to-neutral source voltage and rectifier input voltage of phase A from simulation and experiment, respectively. The fundamental component of the rectifier input voltage determines the load angle and here the load angle and the magnitude of the rectifier input voltage are adjusted to their appropriate values. In experimental result, the voltage level does not go to zero level as it changes between 0 and 120 volts in theoretical one because the sampling rate of the scope was not good enough.

Figure 5.7 and 5.8 show line-to-neutral source voltage and command voltage of phase A from simulation and experiment, respectively. The shape of the generated command voltage is close to sine wave and the load angle can be seen more clearly. Its value is measured around 18 degrees.

Figure 5.9 and 5.10 show the relation between line current and command current of phase A, which are obtained from simulation and experiment, respectively. There is a phase delay of around 7 degrees between them in experimental result because of switching delay as mentioned before.

Figure 5.11 and 5.12 show line currents of all phases from simulation and experiment, respectively. All the phase currents are sinusoidal and the circuit is balanced.

Figure 5.13 and 5.14 show the transient waveform of dc output voltage, which are obtained from simulation and experiment, respectively, for a load change of 100 percent. The dc output voltage decreases by 3 percent during the transient taking place around 160ms.

Figure 5.15 and 5.16 show the transient waveforms of line current of phase A from simulation and experiment, respectively. The load change is the same as above.

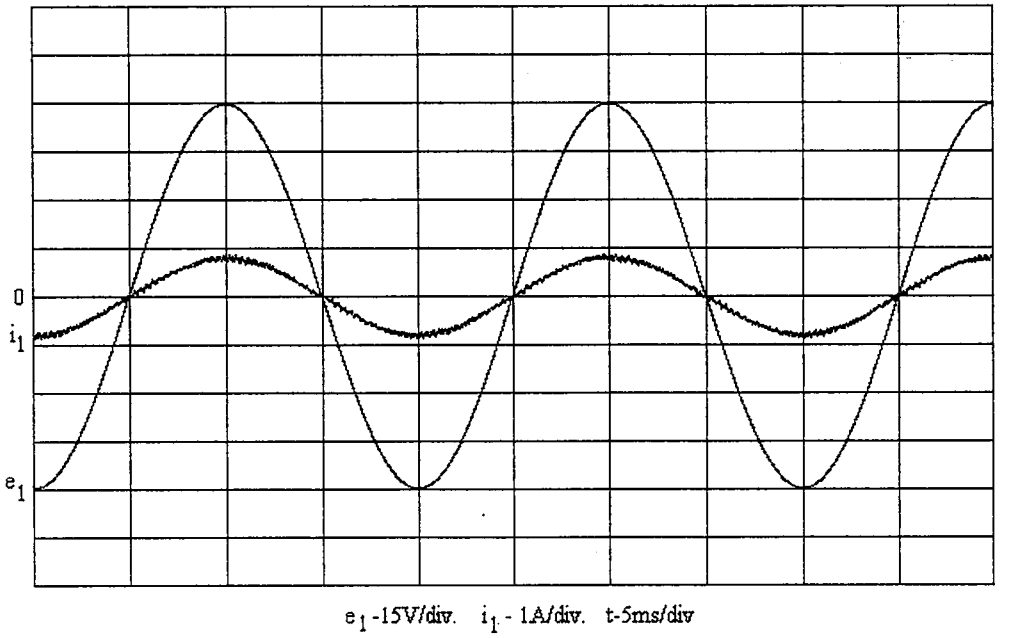


Figure 5.1 Line-to-neutral voltage and line current of phase A (from simulation)

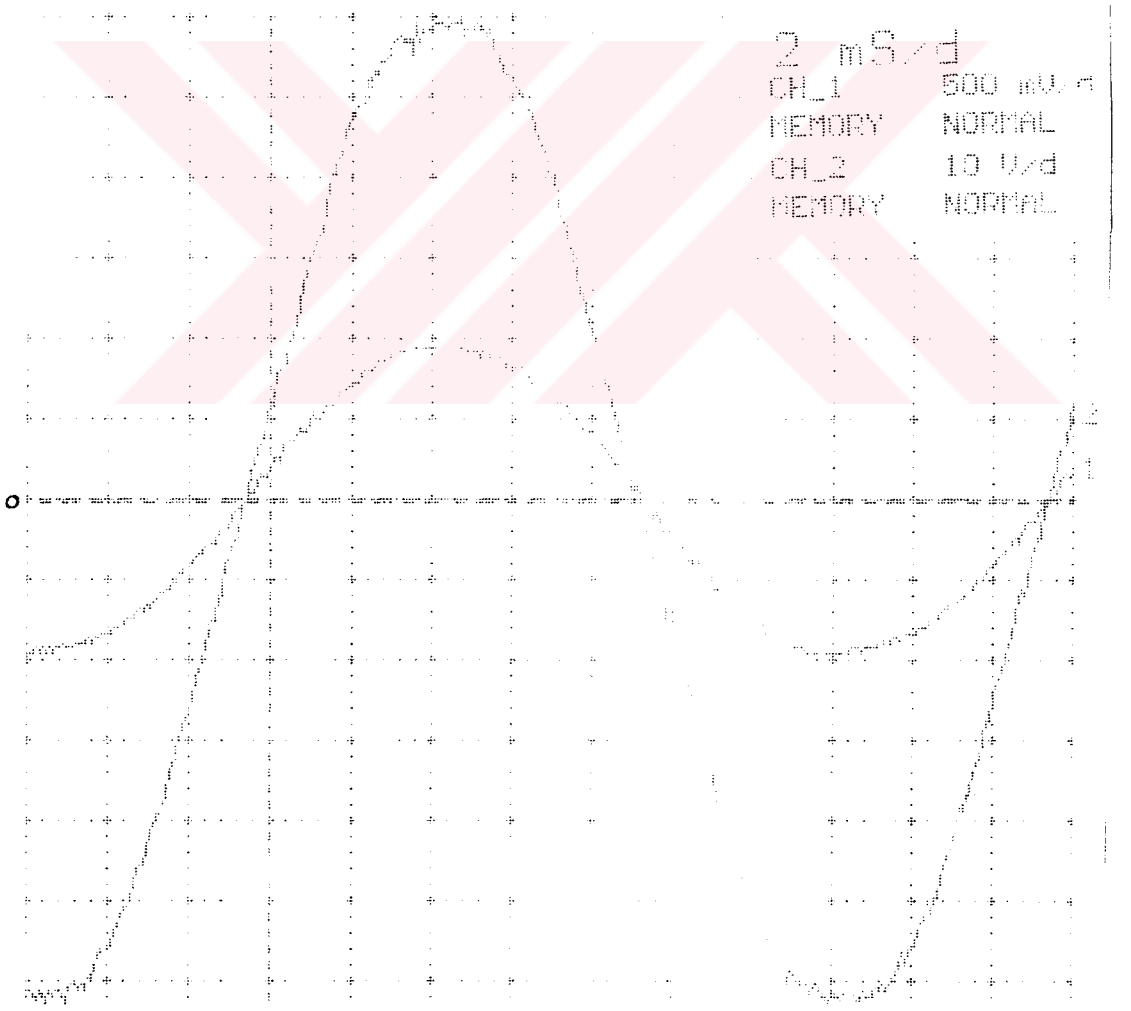


Figure 5.2 Line-to-neutral voltage and line current of phase A (from experiment)

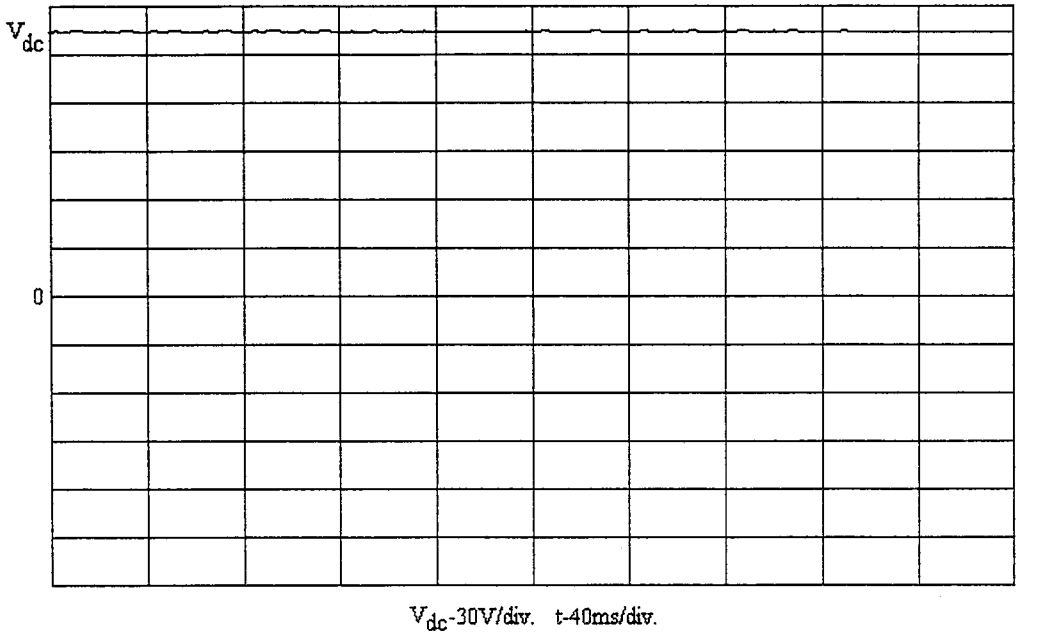


Figure 5.3 Dc output voltage (from simulation)

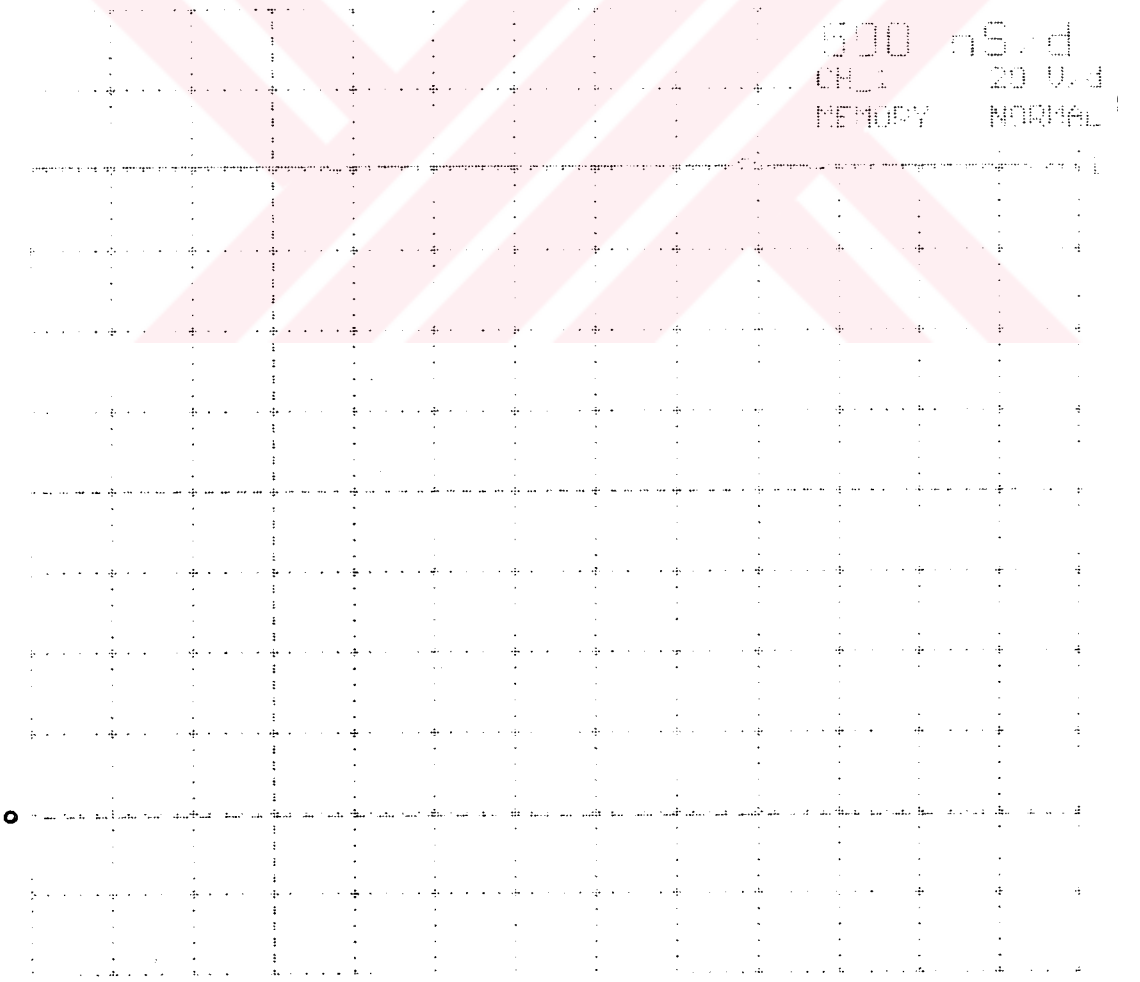


Figure 5.4 Dc output voltage (from experiment)

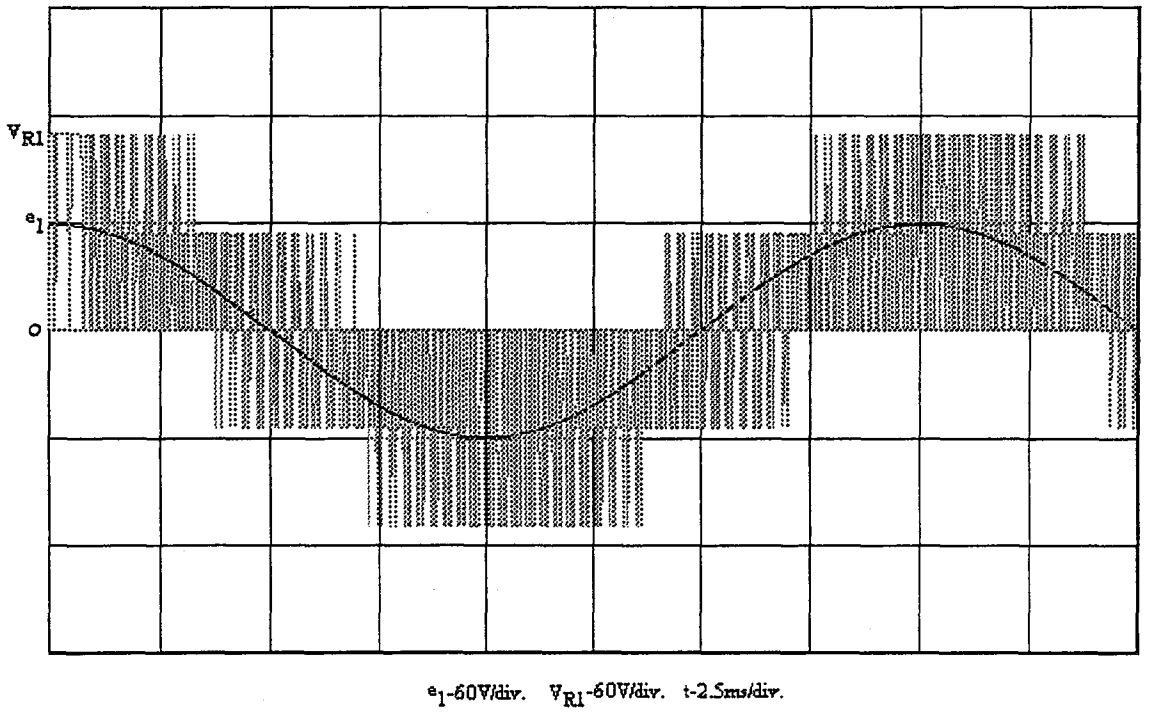


Figure 5.5 Line-to-neutral and rectifier input voltage of phase A (from simulation)

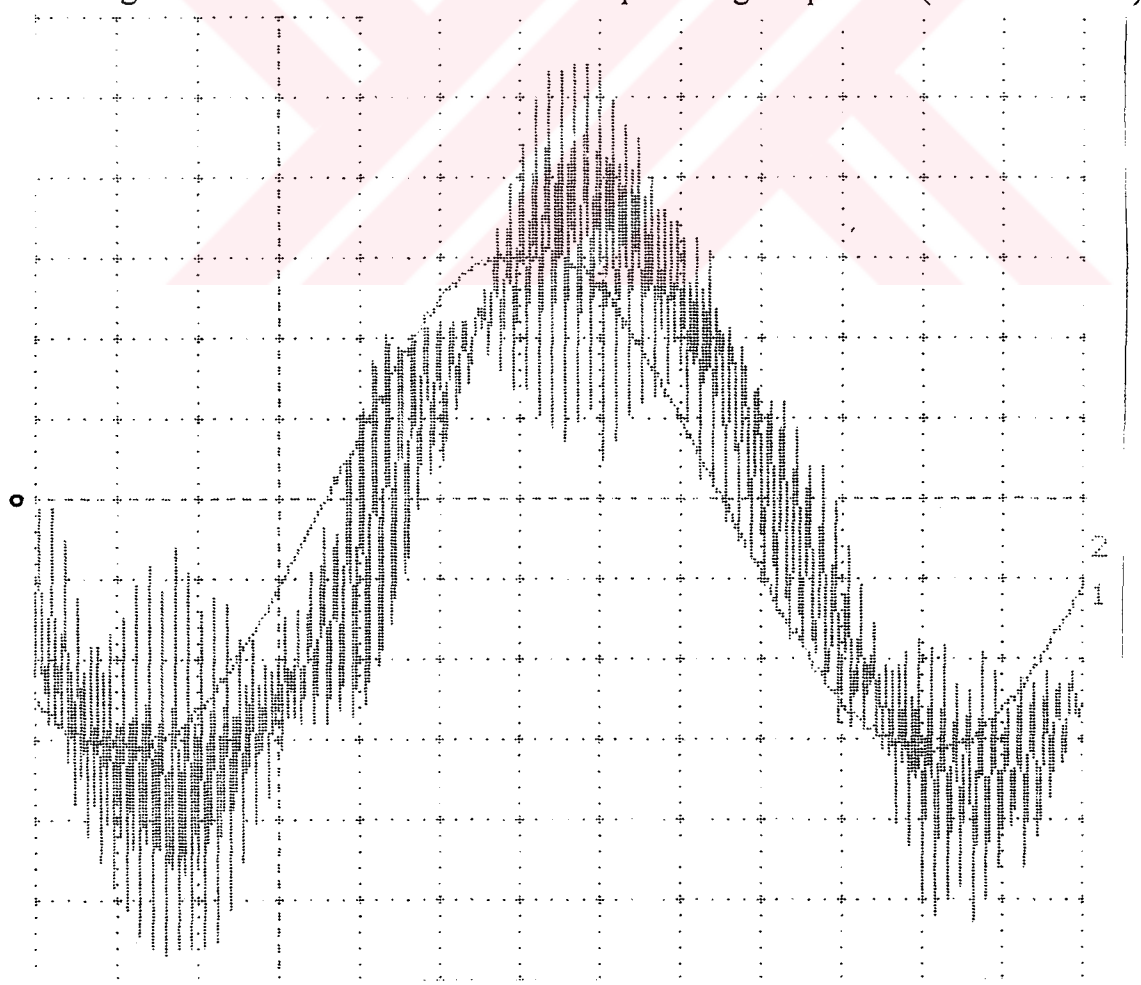


Figure 5.6 Line-to-neutral and rectifier input voltage of phase A (from experiment)

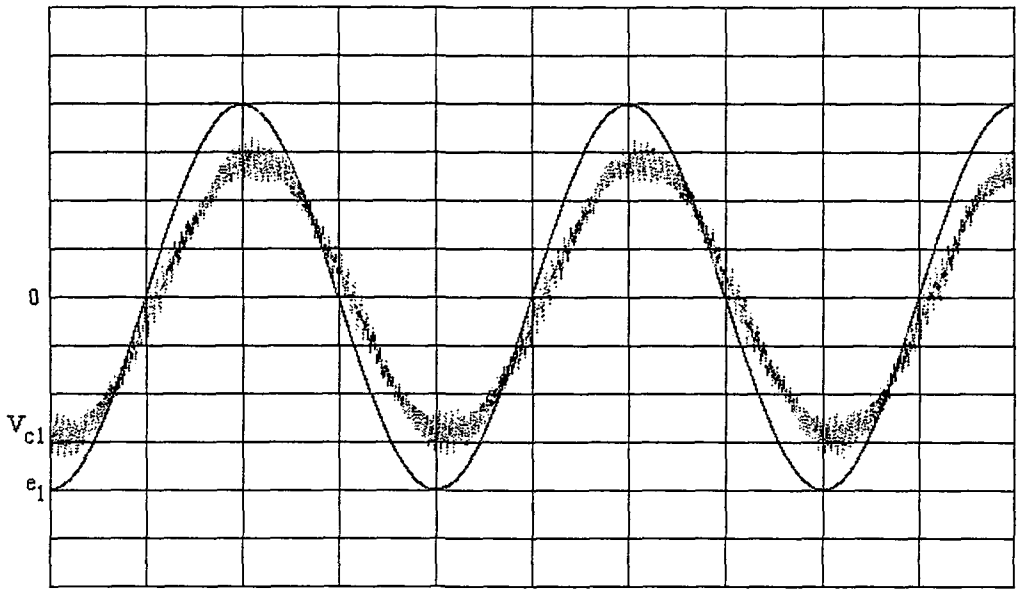


Figure 5.7 Line-to-neutral and command voltage of phase A (from simulation)

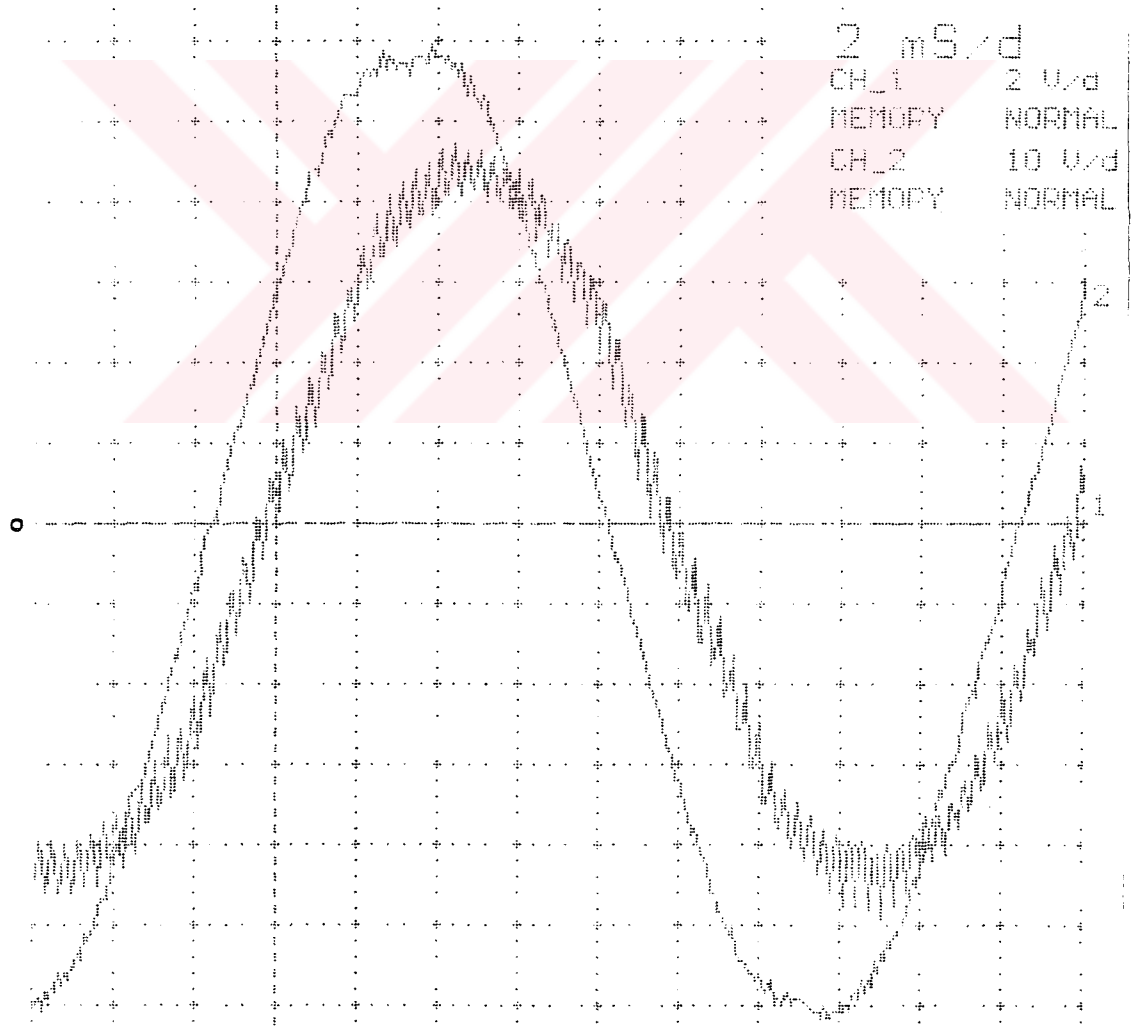


Figure 5.8 Line-to-neutral and command voltage of phase A (from experiment)

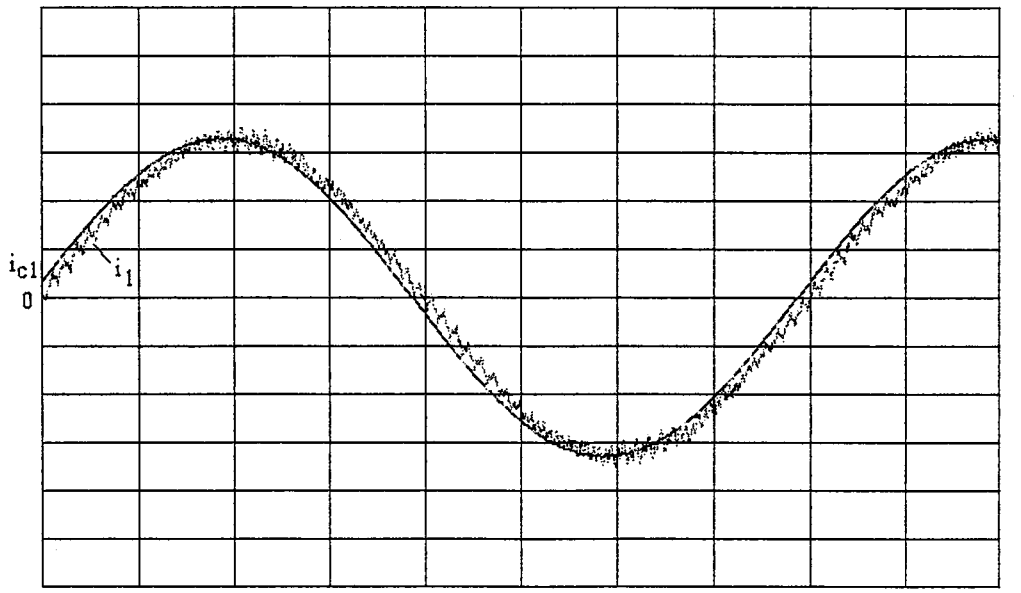


Figure 5.9 Line current and command current of phase A (from simulation)

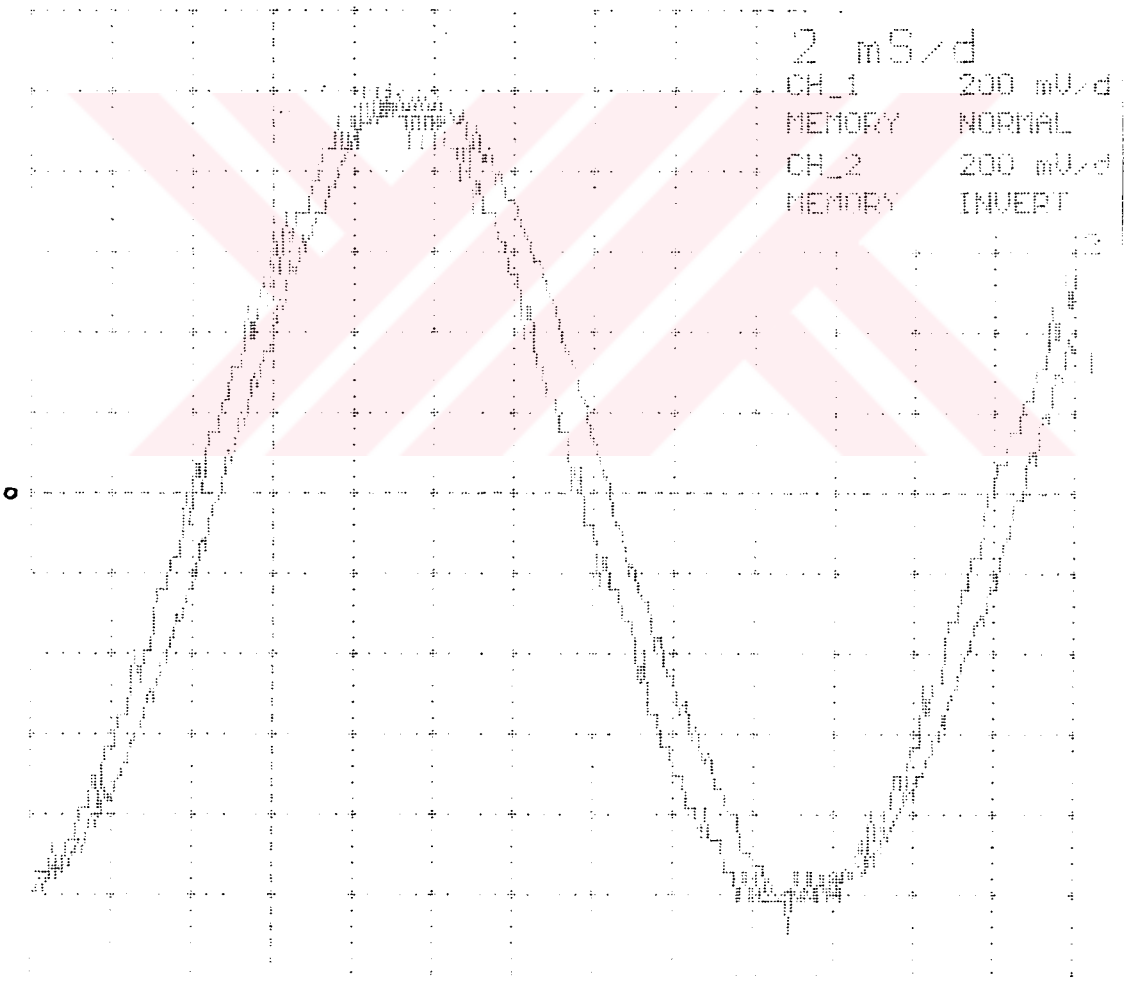


Figure 5.10 Line current and command current of phase A (from experiment)

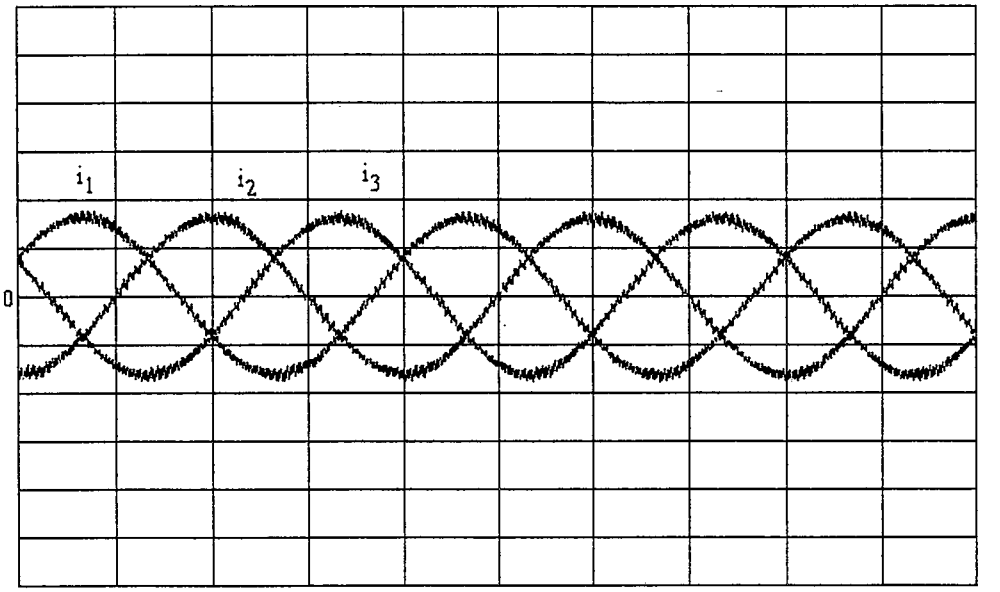


Figure 5.11 Line currents of all phases (from simulation)

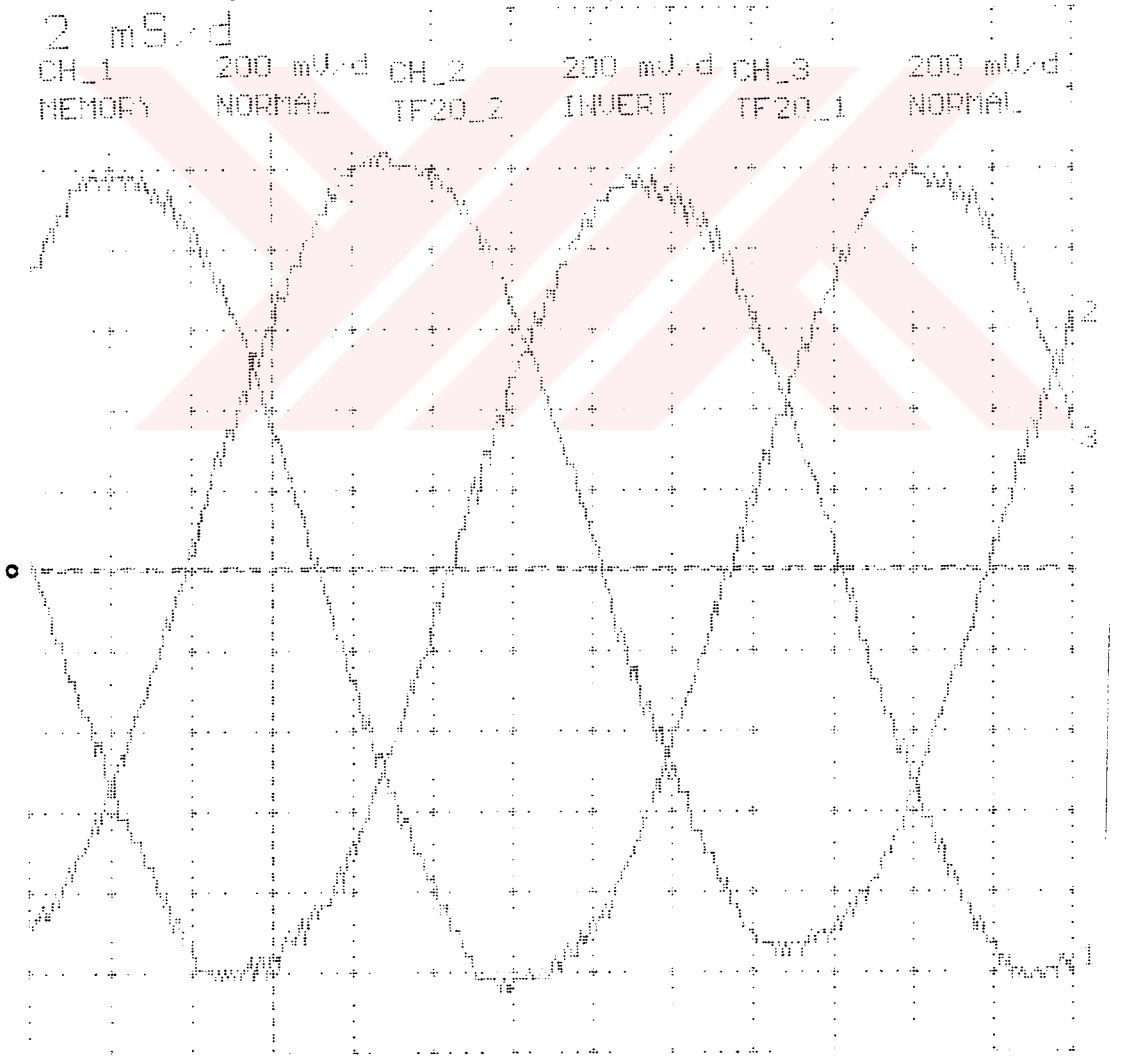


Figure 5.12 Line currents of all phases (from experiment)

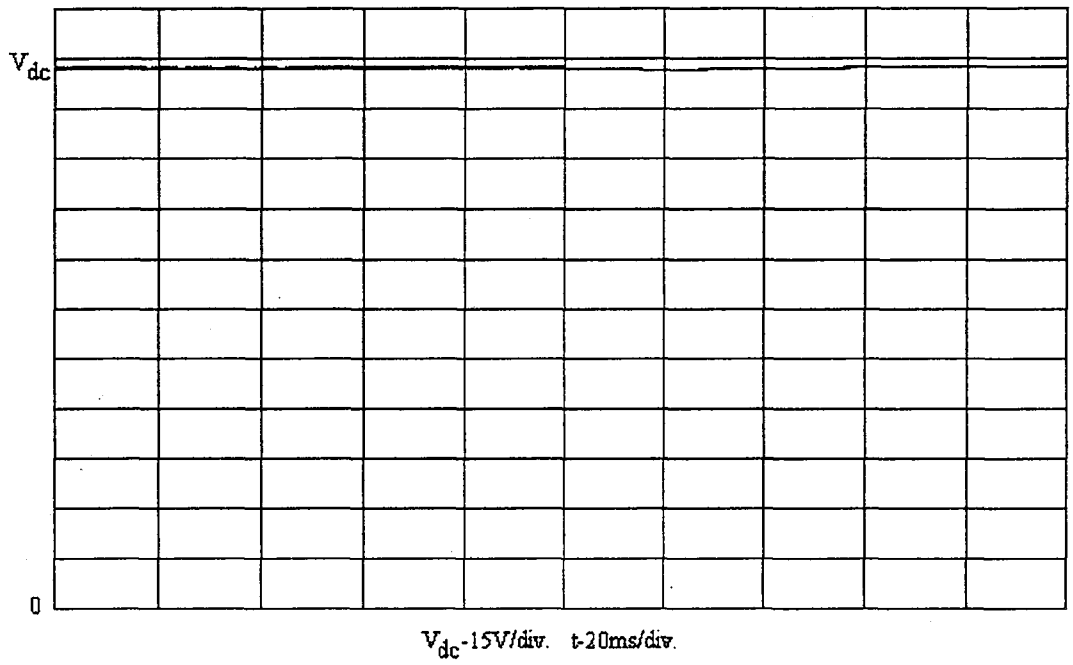


Figure 5.13 Transient waveform of dc output voltage during the change of R_0 from 384 ohms to 192ohms (from simulation)

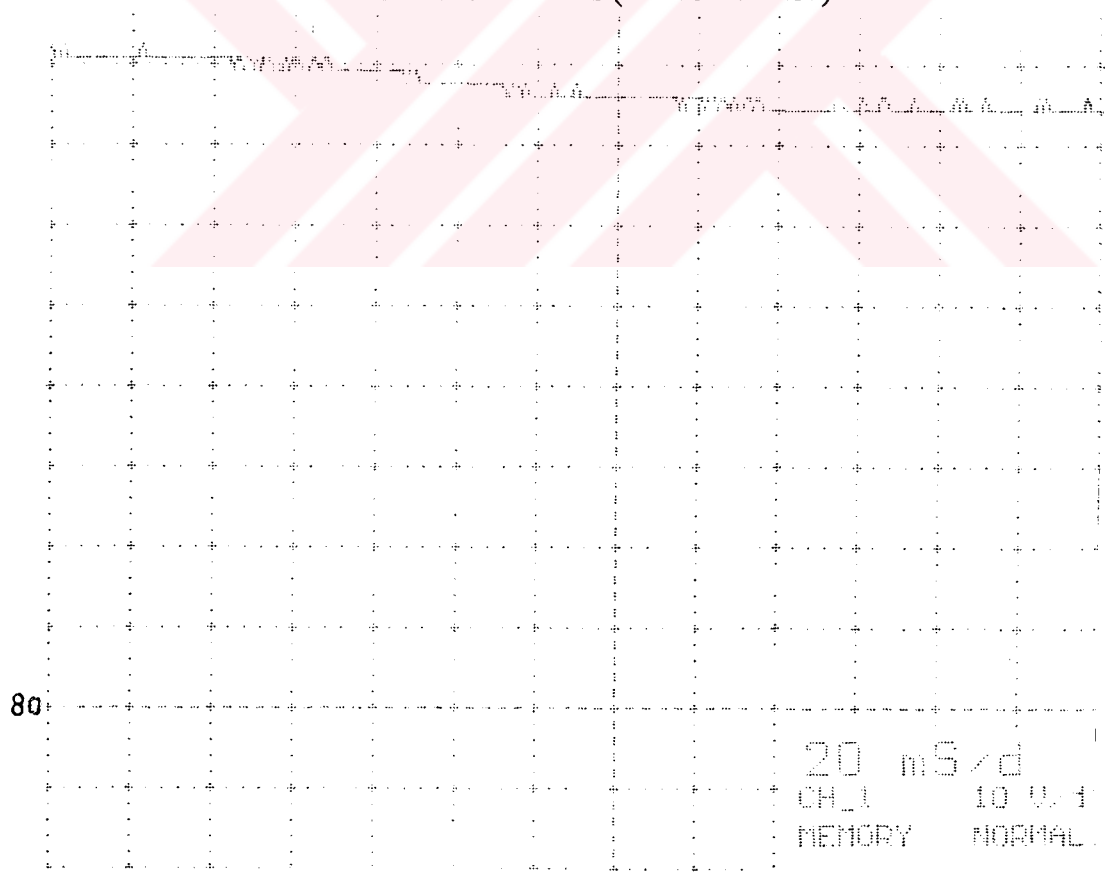


Figure 5.14 Transient waveform of dc output voltage during the change of R_0 from 384 ohms to 192ohms (from experiment)

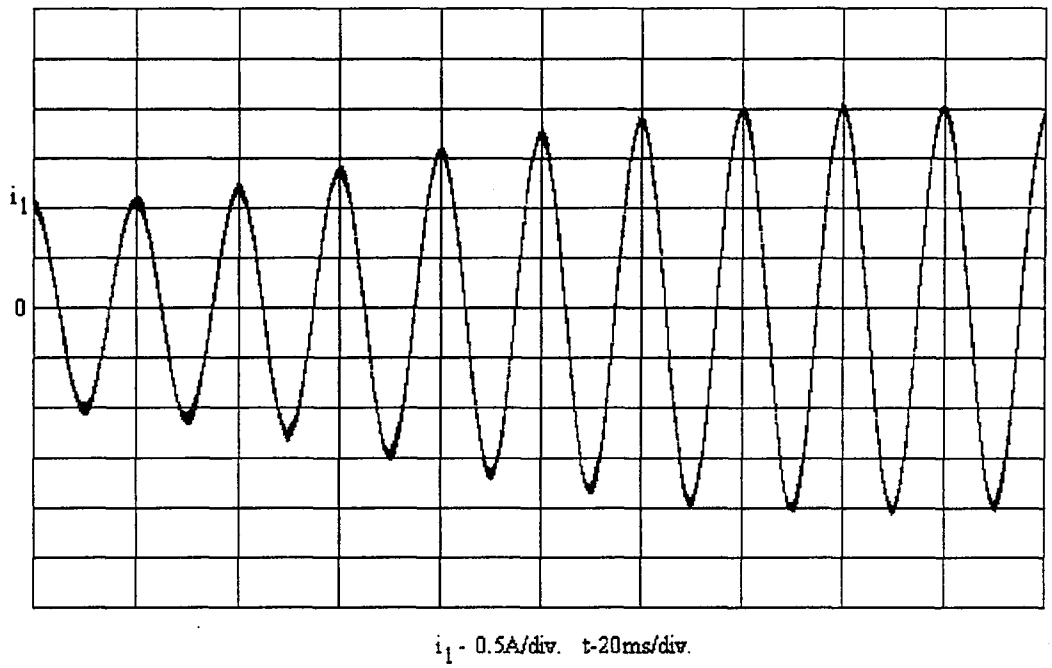


Figure 5.15 Transient waveform of line current of phase A during the change of R_0 from 384ohms to 192ohms (from simulation)

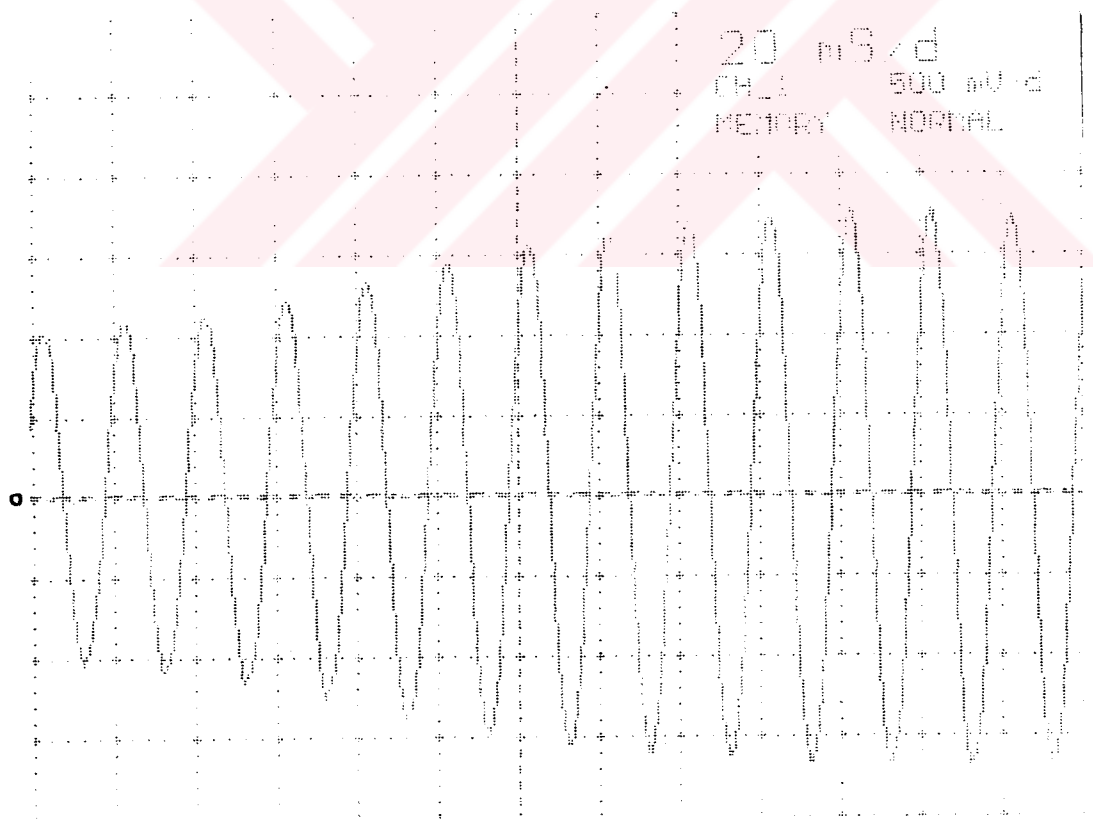


Figure 5.16 Transient waveform of line current of phase A during the change of R_0 from 384ohms to 192ohms (from experiment)

CHAPTER SIX
CONCLUSIONS

A 3-phase PWM rectifier circuit under the predicted current control with fixed switching frequency has been theoretically described and implemented. While describing the circuit, the dedicated simulation program has been mostly made use of. The results of the simulation program have been experimentally verified.

The current waveforms that the rectifier circuit draws from the supply are nearly sinusoidal at unity power factor. They have very low harmonic content at switching frequency. The main purpose of the circuit was to obtain sinusoidal line current at unity power factor and it has been achieved.

The circuit can tolerate load changes. It has a fast dynamic response and can maintain the line currents sinusoidal at unity power factor. However, the regulation is a little decayed depending on the load variation. To overcome this problem, the parameters of the PI controller should be readjusted. This requires an adaptive control.

The circuit can be operated in regenerative mode. Also leading power factor adjustment can be done. This can be achieved by a slight modification on the control circuit. This feature allows the circuit to be used as a reactive power compensator.

The stability region of the rectifier depends on the system parameters. For very extreme changes of the parameters in the system may cause to instability. As mentioned above, an adaptive controller can overcome this problem. However, the control circuit designed for a fixed operation point can tolerate the parameter changes to an extent as it has been verified with a 100 percent load change.

REFERENCES

DIXON, J.W., & OOI, B.T. (1988). Indirect Current Control of a Unity Power Factor Sinusoidal Current Boost type Three-phase Rectifier. IEEE Transactions on Industrial Electronics, 35, no.4, 508-515.

KREYSZIG, E. (1993). Advanced Engineering Mathematics (7^{th} edition). Singapore: John Wiley & Sons, Inc.

LANDER, C.W. (1993). Power Electronics (3^{rd} edition). Singapore: McGraw-Hill

MOHAN, N., UNDELAND, T.M., & ROBBINS, W.P. (1995). Power Electronics: Converters, Applications, and Design (2^{nd} edition).USA: John Wiley & Sons, Inc.

OOI, B.T., SALMON, J.C., DIXON, J.W., & KULKARNI, A.B. (1987). A three-phase Controlled-Current PWM Converter with Leading Power Factor. IEEE Transactions on Industry Applications, IA-23, no.1, 78-84.

PAN, C.T., & CHEN, T.C. (1993). Modelling and analysis of a three phase PWM AC-DC converter without current sensor. IEE Proceedings-B, 140, no.3, 201 -208.

PRAVADALIOĞLU, S. (1995). Kişisel bilgisayar (P.C.) ile üç fazlı bir asenkron motorun PWM yöntemiyle ve geri beslemeli olarak hızını kontrol eden dijital bir sistemin gerçekleştirilmesi ve oluşan harmoniklerin incelenmesi. Yıldız Teknik Üniversitesi Doktora Tezi.

RASHID, M.H. (1988). Power Electronics: Circuits, Devices and Applications. USA: Prentice-Hall, Inc.

RIM, G.H., KIM, W.H., & KANG, I. (1995) A Simplified Analog Controller for Power Factor Correction Converters. IEEE Transactions on Industrial Electronics, 42, no.4, 417-419.

WILLIAMS, B.W. (1992). Power Electronics: Devices, Drivers, Applications, and Passive Components (2nd edition). USA:McGraw-Hill, Inc.

WU, R., DEWAN, S.B., & SLEMON, G.R. (1991). Analysis of a PWM ac to dc Voltage Source Converter Under the Predicted Current Control with a Fixed Switching Frequency. IEEE Transactions on Industry Applications, 27, no.4, 756-764.

WU, R., DEWAN, S.B., & SLEMON, G.R. (1990). A PWM ac-to-dc Converter with Fixed Switching Frequency. IEEE Transactions on Industry Applications, 26, no.5, 880-885.

WU, R., DEWAN, S.B., & SLEMON, G.R. (1991). Analysis of an ac-to-dc Voltage Source Converter Using PWM with Phase and Amplitude Control. IEEE Transactions on Industry Applications, 27, no.2, 355-364.

WU, R., DEWAN, S.B., & SLEMON, G.R. (1987). A Microprocessor based Dual PWM Converter Fed Four-quadrant ac Drive System. IEEE Industrial Applications Society, Annual Meeting, 755-759.

ZARGARI, N.R., & JOOS, G. (1995). Performance Investigation of a Current-Controlled Voltage-Regulated PWM rectifier in Rotating and Stationary Frames. IEEE Transactions on Industrial Electronics, 42, no.4, 396-401.

APPENDIX A

THIS COMPUTER PROGRAM THAT SIMULATES THE CIRCUIT OBTAINS OUTPUTS AND STORE THEM IN DATA FILES.

```
CC    ------------------------------------------------------------
CC                        PROGRAM CLOSED.FOR
CC    ------------------------------------------------------------

CC    PROGRAM MAIN

      Real*4      t,e(4),x(5),ic(3),d(3),Vc(3),Vs,Vrecin(3)
      Real*4      W,pi
      Real*4      R,Ls,C,r0
      Real*4      Ts
      Real*4      THC
      Real*4      Vref,err,icm,yd
      Real*4      tdum


      Common      /ts1/W,pi
      Common      /ts2/R,Ls,C,r0
      Common      /ts3/Ts
      Common      /ts4/THC
      Common      /ts5/Vref,err,icm,yd
      Common      /ts6/tdum
```

```
Open(1,FILE='e1.plo')
Open(2,FILE='e2.plo')
Open(3,FILE='e3.plo')
Open(4,FILE='e4.plo')
Open(5,FILE='ic1.plo')
Open(6,FILE='ic2.plo')
Open(7,FILE='ic3.plo')
Open(8,FILE='d1.plo')
Open(9,FILE='d2.plo')
Open(10,FILE='d3.plo')
Open(11,FILE='i1.plo')
Open(12,FILE='i2.plo')
Open(13,FILE='i3.plo')
Open(14,FILE='vd.plo')
Open(15,FILE='id.plo')
Open(16,FILE='vcc1.out')
Open(17,FILE='vcc2.out')
Open(18,FILE='vcc3.out')
Open(19,FILE='vrrin1.out')
Open(20,FILE='vrrin2.out')
Open(21,FILE='vrrin3.out')

tdum=0.0
k=0
yd=0.

pi=4*atan(1)
W=2*pi*50.

R=2.4
Ls=45e-3
C=4500e-6
```

```
r0=384.
Ts=0.32e-3
THC=5.74*pi/180.0

Vref=165.

x(1)=0.87*cos(0.)
x(2)=0.87*cos(-2*pi/3)
x(3)=0.87*cos(2*pi/3)
x(4)=165.
x(5)=0.

write(*,*) 'Running...'

DO 100 t=0.0,0.4,1e-5

if (t.ge.0.2) then
r0=192.
else
r0=384.
end if

err=Vref-x(4)
yd=(x(4)-e(4))/r0

write(15,*) t,yd

call   Inputs(t,e)
write(1,*) t,e(1)
write(2,*) t,e(2)
write(3,*) t,e(3)
write(4,*) t,e(4)
```

```
      call   CurrentCom(t,ic,x)
      write(5,*) t,ic(1)
      write(6,*) t,ic(2)
      write(7,*) t,ic(3)

      call   Switches(t,x,e,d)
      write(8,*) t,d(1)
      write(9,*) t,d(2)
      write(10,*) t,d(3)

      write(11,*) t,x(1)
      write(12,*) t,x(2)
      write(13,*) t,x(3)
      write(14,*) t,x(4)

      call   CurrentVolt(t,x,e,Vc)
      write(16,*) t,vc(1)
      write(17,*) t,vc(1)
      write(18,*) t,vc(1)

      call   Switches(t,e,x,d)
      vrecin(1)=d(1)*x(4)+x(1)*0.6-x(4)*(d(1)+d(2)+d(3))/3
      vrecin(2)=d(2)*x(4)+x(2)*0.6-x(4)*(d(1)+d(2)+d(3))/3
      vrecin(3)=d(3)*x(4)+x(3)*0.6-x(4)*(d(1)+d(2)+d(3))/3
      write(19,*) t,Vrecin(1)
      write(20,*) t,Vrecin(2)
      write(21,*) t,Vrecin(3)

      CALL   RKSYST(x,t)

100   CONTINUE
```

```
      close(1)
      close(2)
      close(3)
      close(4)
      close(5)
      close(6)
      close(7)
      close(8)
      close(9)
      close(10)
      close(11)
      close(12)
      close(13)
      close(14)
      close(15)
      close(16)
      close(17)
      close(18)
      close(19)
      close(20)
      close(21)

      END

CC    ------------------------------------------------------------
      Subroutine    RKSYST(x,t)
CC    ------------------------------------------------------------

      Real*4        x(5),e(4),d(3),xdot(5),xend(4),xwrk(4,5),h,t
      Integer i
```

```
      h=1e-5
      CALL      Inputs(t,e)
      CALL      Switches(t,x,e,d)
      CALL      Derivatives(x,e,d,xdot)

      Do 10 i=1,5
      xwrk(1,i)=h*xdot(i)
      xend(i)=x(i)+xwrk(1,i)/2.0
10    Continue

      CALL      Inputs(t+h/2.0,e)
      CALL      Switches(t,x,e,d)
      CALL      Derivatives(xend,e,d,xdot)

      Do 20 i=1,5
      xwrk(2,i)=h*xdot(i)
      xend(i)=x(i)+xwrk(2,i)/2.0
20    Continue

      CALL      Inputs(t+h/2.0,e)
      CALL      Switches(t,x,e,d)
      CALL      Derivatives(xend,e,d,xdot)

      Do 30 i=1,5
      xwrk(3,i)=h*xdot(i)
      xend(i)=x(i)+xwrk(3,i)
30    Continue

      CALL      Inputs(t+h,e)
      CALL      Switches(t,x,e,d)
      CALL      Derivatives(xend,e,d,xdot)
```

```
      Do 40 i=1,5
      xwrk(4,i)=h*xdot(i)
40    Continue

      Do 50 i=1,5
      xend(i)=x(i)+(xwrk(1,i)+2.0*xwrk(2,i)+2.0*xwrk(3,i)+xwrk(4,i))/6.0
      x(i)=xend(i)
50    Continue

      Return
      End

CC    ------------------------------------------------------------
      Subroutine     Derivatives(x,e,d,xdot)
CC    ------------------------------------------------------------

      Real*4         x(5),e(4),d(3),xdot(5)
      Real*4         R,Ls,C,r0
      Real*4         Vref,err,icm,yd

      common         /ts2/R,Ls,C,r0
      common         /ts5/Vref,err,icm,yd

      xdot(1)=(-R*x(1)-(d(1)-(d(1)+d(2)+d(3))/3)*x(4)+e(1))/Ls
      xdot(2)=(-R*x(2)-(d(2)-(d(1)+d(2)+d(3))/3)*x(4)+e(2))/Ls
      xdot(3)=(-R*x(3)-(d(3)-(d(1)+d(2)+d(3))/3)*x(4)+e(3))/Ls
      xdot(4)=(d(1)*x(1)+d(2)*x(2)+d(3)*x(3)-x(4)/r0+e(4)/r0)/C
      xdot(5)=55.6*err

      Return
      End
```

```
CC    ------------------------------------------------------------
      Subroutine    Inputs(t,e)
CC    ------------------------------------------------------------

      Real*4        t,e(4),a
      Real*4        W,pi

      common        /ts1/W,pi

      e(1)=60*cos(W*t)
      e(2)=60*cos(W*t-2*pi/3)
      e(3)=60*cos(W*t+2*pi/3)
      e(4)=0.

      Return
      End

CC    ------------------------------------------------------------
      Subroutine    Switches(t,x,e,d)
CC    ------------------------------------------------------------

      Real*4        t,x(5),e(4),Vs,Vc(3),d(3)
      Integer       m

      CALL          CurrentVolt(t,x,e,Vc)
      CALL          Triangle(t,Vs)

      Do 15 m=1,3
      if (Vs.le.Vc(m)) then
      d(m)=1.
      else
      d(m)=0.
```

```
      end if
15    Continue

      Return
      End

CC    ------------------------------------------------------------
      Subroutine     CurrentCom(t,ic,x)
CC    ------------------------------------------------------------

      Real*4         t,ic(3),x(5)
      Real*4         W,pi
      Real*4         THC
      Real*4         Vref,err,icm,yd

      common          /ts1/W,pi
      common          /ts4/THC
      common          /ts5/Vref,err,icm,yd

      icm=(1*err+x(5))
      if (icm.ge.15.) then
      icm=15.
      else
      icm=icm
      end if

      ic(1)=icm*cos(W*t+THC)
      ic(2)=icm*cos(W*t+THC-2*pi/3)
      ic(3)=icm*cos(W*t+THC+2*pi/3)

      Return
      End
```

```
CC    ------------------------------------------------------------
      Subroutine     CurrentVolt(t,x,e,Vc)
CC    ------------------------------------------------------------

      Real*4         t,x(5),e(4),ic(3),Vc(3)
      Real*4         R,Ls,C,r0
      Real*4         Ts
      Real*4         Vref,err,icm,yd

      common         /ts2/R,Ls,C,r0
      common         /ts3/Ts
      common         /ts5/Vref,err,icm,yd

      CALL           CurrentCom(t,ic,x)

      Vc(1)=20*(e(1)-(R-Ls/Ts)*x(1)-(Ls/Ts)*ic(1))/Vref
      Vc(2)=20*(e(2)-(R-Ls/Ts)*x(2)-(Ls/Ts)*ic(2))/Vref
      Vc(3)=20*(e(3)-(R-Ls/Ts)*x(3)-(Ls/Ts)*ic(3))/Vref

      Return
      End

CC    ------------------------------------------------------------
      Subroutine     Triangle(t,Vs)
CC    ------------------------------------------------------------

      Real*4         t,Vs
      Real*4         Ts,tdum
      Integer        k

      common         /ts3/Ts
      common         /ts6/tdum
```

```
      tdum=t-k*Ts

      if(tdum.ge.Ts) then
      k=k+1
      tdum=t-k*Ts
      else
      tdum=tdum
      end if

      if(tdum.le.Ts/2) then
      Vs=10-40*tdum/Ts
      else
      Vs=-30+40*tdum/Ts
      end if

      Return
      End

CC    ------------------------------------------------------------
CC    ------------------------------------------------------------
```

THIS PROGRAM READS STORED DATA FILES AND DRAWS GRAPHICAL WAVEFORMS OF THEM.

```
CC    ------------------------------------------------------------
CC    -              PROGRAM DRCLOSED.FOR              -
CC    ------------------------------------------------------------

CC    PROGRAM MAIN

      Include 'fgraph.fi'
      Include 'fgraph.fd'

      call graphicsmode()
      call drawlines()
      call drawplots()



CC    ------------------------------------------------------------
      SUBROUTINE graphicsmode()
CC    ------------------------------------------------------------

      Include 'fgraph.fd'

      integer*2      modestatus,maxx,maxy
      record/videoconfig/myscreen

      common maxx,maxy

      modestatus=setvideomode($maxresmode)
      if (modestatus.eq.0) stop 'error:cannot set graphics mode'
```

```
      call getvideoconfig(myscreen)
      maxx=myscreen.numxpixels-1
      maxy=myscreen.numypixels-1

      END


CC    ------------------------------------------------------------
      SUBROUTINE drawlines()
CC    ------------------------------------------------------------

      Include 'fgraph.fd'

      Integer*2      status,maxx,maxy,i,j
      Record/xycoord/xy
      Record/rccoord/curpos

      Common         maxx,maxy

      CALL clearscreen($gclearscreen)
      CALL setvieworg(0,0,xy)
      status=setcolor(8)
      status=rectangle($gborder,40,60,maxx,maxy-59)

      CALL   setvieworg(40,240,xy)

      Do 10 j=-150,150,30

      CALL moveto(0,j,xy)
      status=lineto(600,j)

10    Continue
```

```
      Do 20 i=0,600,60

      CALL moveto(i,-180,xy)
      status=lineto(i,180)

20    Continue

      END

CC    ------------------------------------------------------------
      SUBROUTINE drawplots()
CC    ------------------------------------------------------------

      Include 'fgraph.fd'

      Integer*2      status,i,j
      Real*4  x,y,a,b
      Record/xycoord/xy

      open(1,FILE='e1.plo',status='old')
      open(4,FILE='i1.plo',status='old')
      open(7,FILE='vd.plo',status='old')

      Do 5 i=0,3

      CALL drawlines()
      CALL setvieworg(40,240,xy)

      do 10 j=1,20000
```

```
      status=setcolor(2)

      read(1,*) x,y
      CALL setvieworg(40,240,xy)
      CALL moveto(0,0,xy)
      status=setpixel((x-4*0.05)*3000,-y*2)

      status=setcolor(4)

      read(4,*) x,y
      CALL setvieworg(40,240,xy)
      CALL moveto(0,0,xy)
      status=setpixel((x-4*0.05)*3000,-y*30)

      status=setcolor(6)

      read(7,*) x,y
      CALL setvieworg(40,240,xy)
      CALL moveto(0,0,xy)
      status=setpixel((x-i*0.05)*12000,-y*60)

10    Continue

      read(*,*)

5     Continue

      END

CC    ------------------------------------------------------------
CC    ------------------------------------------------------------
```

APPENDIX B

International
IOR Rectifier

Preliminary Data Sheet PD - 9.1115

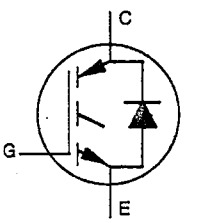
IRGPH30MD2

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated Fast CoPack IGBT

Features

- Short circuit rated -10µs @125°C, V_{GE} = 15V
- Switching-loss rating includes all "tail" losses
- HEXFRED™ soft ultrafast diodes
- Optimized for medium operating frequency (1 to 10kHz)



n-channel

V_{CES} = 1200V

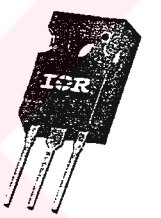
$V_{CE(sat)} \leq 3.5V$

@V_{GE} = 15V, I_C = 9.0A

Description

Co-packaged IGBTs are a natural extension of International Rectifier's well known IGBT line. They provide the convenience of an IGBT and an ultrafast recovery diode in one package, resulting in substantial benefits to a host of high-voltage, high-current, applications.

These new short circuit rated devices are especially suited for motor control and other applications requiring short circuit withstand capability.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	15	A
I_C @ T_C = 100°C	Continuous Collector Current	9.0	
I_{CM}	Pulsed Collector Current ①	30	
I_{LM}	Clamped Inductive Load Current ②	30	
I_F @ T_C = 100°C	Diode Continuous Forward Current	6.0	
I_{FM}	Diode Maximum Forward Current	30	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	100	W
P_D @ T_C = 100°C	Maximum Power Dissipation	42	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	1.2	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	2.5	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

Revision 2

IRGPH30MD2

IOR

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	—	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	3.1	3.5	V	I_C = 9.0A V_{GE} = 15V
		—	4.9	—		I_C = 15A
		—	3.6	—		I_C = 9.0A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	5.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-14	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	2.5	—	—	S	V_{CE} = 100V, I_C = 9.0A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.7	3.0	V	I_C = 6.0A
		—	2.4	2.7		I_C = 6.0A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	25	30	nC	I_C = 9.0A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	—	6.0		V_{CC} = 960V
Q_{gc}	Gate - Collector Charge (turn-on)	—	—	15		
$t_{d(on)}$	Turn-On Delay Time	—	2.3	—	ns	T_J = 25°C
t_r	Rise Time	—	10	—		I_C = 9.0A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	200	450		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	210	390		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	—	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	—	—		
E_{ts}	Total Switching Loss	—	4.0	7.0		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 23Ω, V_{CPK} < 1000V
$t_{d(on)}$	Turn-On Delay Time	—	33	—	ns	T_J = 150°C,
t_r	Rise Time	—	20	—		I_C = 9.0A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	480	—		V_{GE} = 15V, R_G = 23Ω
t_f	Fall Time	—	450	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	8.0	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	670	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	50	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	10	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	53	80	ns	T_J = 25°C
		—	87	130		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	4.4	8.0	A	T_J = 25°C
		—	5.0	9.0		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	116	320	nC	T_J = 25°C
		—	233	585		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	180	—	A/µs	T_J = 25°C
	During t_b	—	100	—		T_J = 125°C

I_F = 6.0A

V_R = 200V

di/dt = 200A/µs

Notes: ① Repetitive rating; V_{GE}=20V, pulse width limited by max. junction temperature.

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 23Ω

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Refer to Section D - page D-13 for Package Outline 3 - JEDEC Outline TO-247AC

International
IOR Rectifier

Preliminary Data Sheet PD - 9.1118

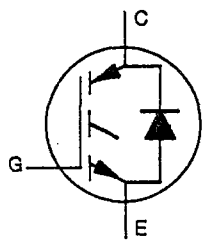
IRGPH40MD2

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRAFAST SOFT RECOVERY DIODE

Short Circuit Rated Fast CoPack IGBT

Features

- Short circuit rated -10µs @125°C, V_{GE} = 15V
- Switching-loss rating includes all "tail" losses
- HEXFRED™ soft ultrafast diodes
- Optimized for medium operating frequency (1 to 10kHz)



n-channel

V_{CES} = 1200V

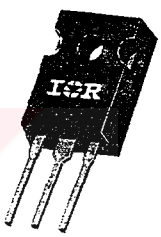
$V_{CE(sat)} \leq$ 3.4V

@V_{GE} = 15V, I_C = 18A

Description

Co-packaged IGBTs are a natural extension of International Rectifier's well known IGBT line. They provide the convenience of an IGBT and an ultrafast recovery diode in one package, resulting in substantial benefits to a host of high-voltage, high-current, applications.

These new short circuit rated devices are especially suited for motor control and other applications requiring short circuit withstand capability.



TO-247AC

Motor Control Fast Co-Packs

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	31	A
I_C @ T_C = 100°C	Continuous Collector Current	18	
I_{CM}	Pulsed Collector Current ①	62	
I_{LM}	Clamped Inductive Load Current ②	62	
I_F @ T_C = 100°C	Diode Continuous Forward Current	8.0	
I_{FM}	Diode Maximum Forward Current	62	
t_{sc}	Short Circuit Withstand Time	10	µs
V_{GE}	Gate-to-Emitter Voltage	± 20	V
P_D @ T_C = 25°C	Maximum Power Dissipation	160	W
P_D @ T_C = 100°C	Maximum Power Dissipation	65	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	0.77	°C/W
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	1.7	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	—	40	
Wt	Weight	—	6 (0.21)	—	g (oz)

Revision 2

IRGPH40MD2

IOR

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage③	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$\Delta V_{(BR)CES}/\Delta T_J$	Temp. Coeff. of Breakdown Voltage	—	1.1	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.3	3.4	V	I_C = 18A V_{GE} = 15V
		—	3.0	—		I_C = 31A
		—	2.8	—		I_C = 18A, T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	5.5		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temp. Coeff. of Threshold Voltage	—	-14	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ④	4.0	10	—	S	V_{CE} = 100V, I_C = 18A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	3500		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
V_{FM}	Diode Forward Voltage Drop	—	2.6	3.3	V	I_C = 8A
		—	2.3	3.0		I_C = 8A, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	50	75	nC	I_C = 18A
Qge	Gate - Emitter Charge (turn-on)	—	11	21		V_{CC} = 400V
Q_{gc}	Gate - Collector Charge (turn-on)	—	15	30		
$t_{d(on)}$	Turn-On Delay Time	—	67	—	ns	T_J = 25°C
t_r	Rise Time	—	89	—		I_C = 18A, V_{CC} =800V
$t_{d(off)}$	Turn-Off Delay Time	—	340	930		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	510	930		Energy losses include "tail" and
E_{on}	Turn-On Switching Loss	—	2.1	—	mJ	diode reverse recovery.
E_{off}	Turn-Off Switching Loss	—	5.9	—		
E_{ts}	Total Switching Loss	—	8.0	13		
t_{sc}	Short Circuit Withstand Time	10	—	—	µs	V_{CC} = 720V, T_J = 125°C
						V_{GE} = 15V, R_G = 10Ω, V_{CPK} < 1000V
$t_{d(on)}$	Turn-On Delay Time	—	64	—	ns	T_J = 150°C,
t_r	Rise Time	—	74	—		I_C = 18A, V_{CC} = 800V
$t_{d(off)}$	Turn-Off Delay Time	—	550	—		V_{GE} = 15V, R_G = 10Ω
t_f	Fall Time	—	1200	—		Energy losses include "tail" and
E_{ts}	Total Switching Loss	—	16	—	mJ	diode reverse recovery.
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	1400	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	100	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	15	—		f = 1.0MHz
t_{rr}	Diode Reverse Recovery Time	—	63	95	ns	T_J = 25°C
		—	106	160		T_J = 125°C
I_{rr}	Diode Peak Reverse Recovery Current	—	4.5	8.0	A	T_J = 25°C
		—	6.2	11		T_J = 125°C
Q_{rr}	Diode Reverse Recovery Charge	—	140	380	nC	T_J = 25°C
		—	335	880		T_J = 125°C
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery	—	133	—	A/µs	T_J = 25°C
	During t_b	—	85	—		T_J = 125°C

I_F = 8A; V_R = 200V; di/dt = 200A/µs

Notes: ① Repetitive rating; V_{GE}=20V, pulse width limited by max. junction temperature.

② V_{CC}=80%(V_{CES}), V_{GE}=20V, L=10µH, R_G= 10Ω

③ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

④ Pulse width 5.0µs, single shot.

Refer to Section D - page D-13 for Package Outline 3 - JEDEC Outline TO-247AC

International
IOR Rectifier

Data Sheet No. PD-6.030C

IR2113

HIGH AND LOW SIDE DRIVER

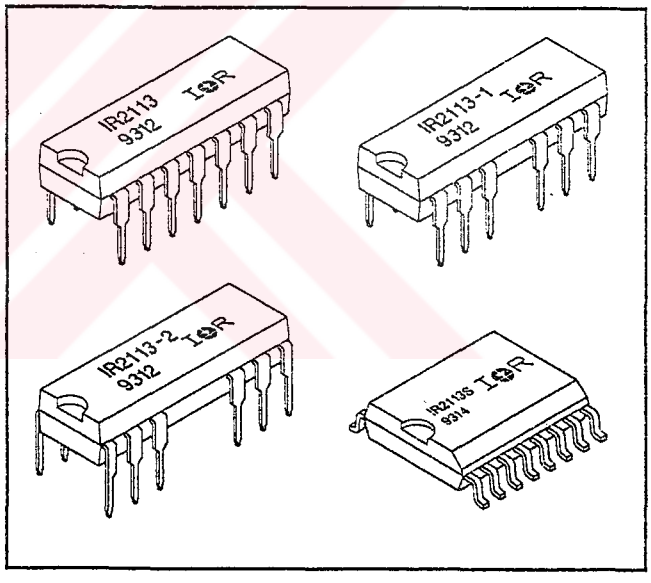
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	600V max.
$I_{O+/-}$	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching	10 ns

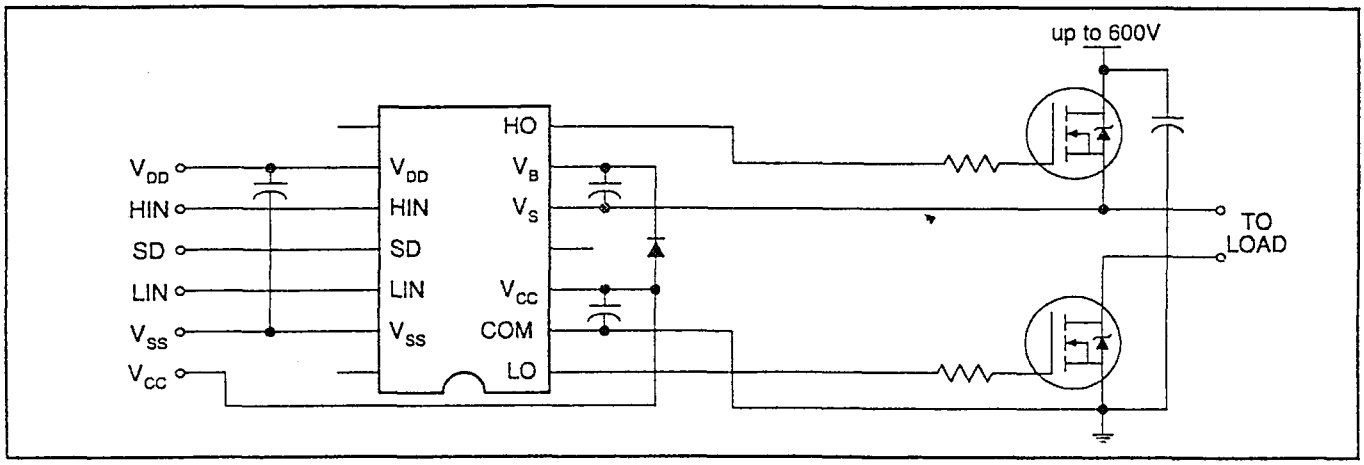
Packages



Description

The IR2113 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	625	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (14 Lead DIP)	—	1.6	W
	(14 Lead DIP w/o Lead 4)	—	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	—	1.6	
	(16 Lead SOIC)	—	1.25	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (14 Lead DIP)	—	75	°C/W
	(14 Lead DIP w/o Lead 4)	—	85	
	(16 Lead DIP w/o Leads 5 & 6)	—	75	
	(16 Lead SOIC)	—	100	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 10	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	Note 1	600	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 5	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

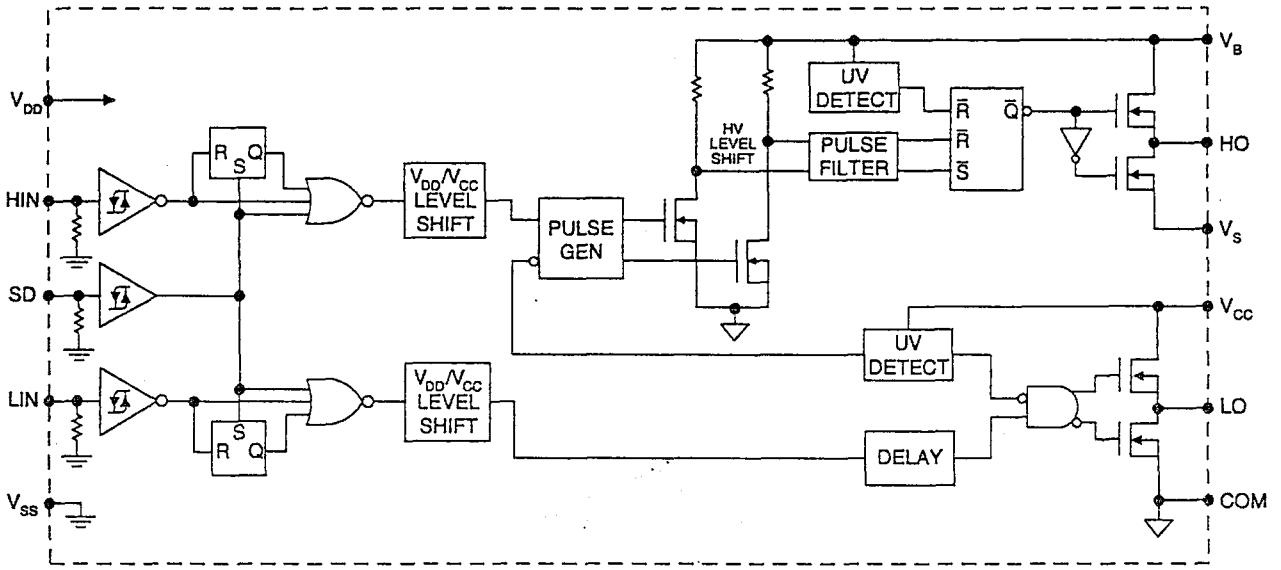
Symbol	Parameter Definition	Figure	Value Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	8	—	94	125		V_S = 600V
t_{sd}	Shutdown Propagation Delay	9	—	110	140		V_S = 600V
t_r	Turn-On Rise Time	10	—	25	35		
t_f	Turn-Off Fall Time	11	—	17	25		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	—	10		Figure 5

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Figure	Value Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	13	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset Supply Leakage Current	16	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" Input Bias Current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	25	7.0	8.2	9.4		
I_{O+}	Output High Short Circuit Pulsed Current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

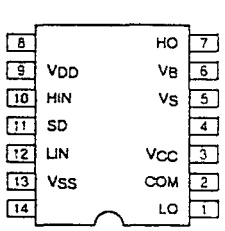
Functional Block Diagram



Lead Definitions

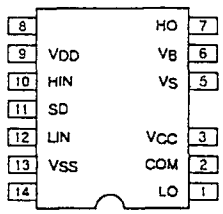
Lead Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



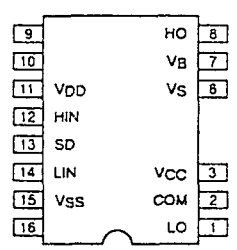
14 Lead DIP

IR2113



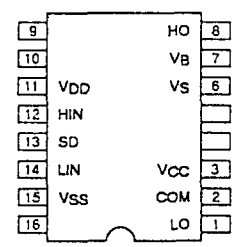
14 Lead DIP w/o Lead 4

IR2113-1



16 Lead DIP w/o Leads 4 & 5

IR2113-2

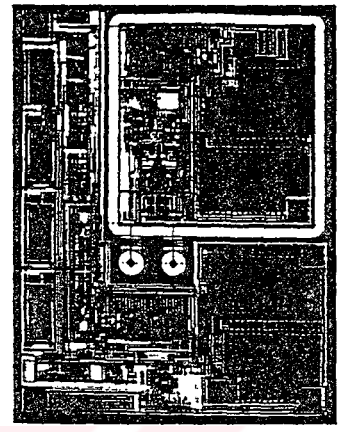


16 Lead SOIC (Wide Body)

IR2113S

Part Number

Device Information

Process & Design Rule		HVDCMOS 4.0 µm
Transistor Count		220
Die Size		98 X 126 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800Å
Connections	Material	Poly Silicon
First Layer	Width	4 µm
	Spacing	6 µm
	Thickness	5000Å
	Material	Al - Si (Si: 1.0% ±0.1%)
Second Layer	Width	6 µm
	Spacing	9 µm
	Thickness	20,000Å
Contact Hole Dimension		8 µm X 8 µm
Insulation Layer	Material	PSG (SiO_2)
	Thickness	1.5 µm
Passivation	Material	PSG (SiO_2)
	Thickness	1.5 µm
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	14 & 16 Lead PDIP / 16 Lead SOIC
	Materials	EME6300 / MP150 / MP190
Remarks:		

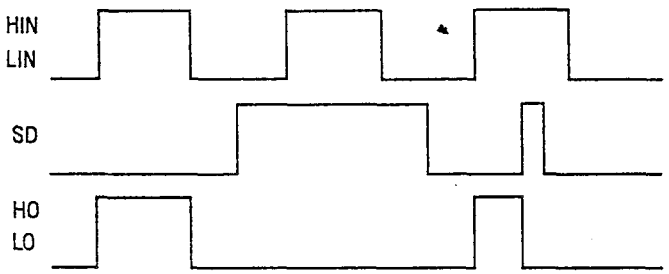


Figure 1. Input/Output Timing Diagram

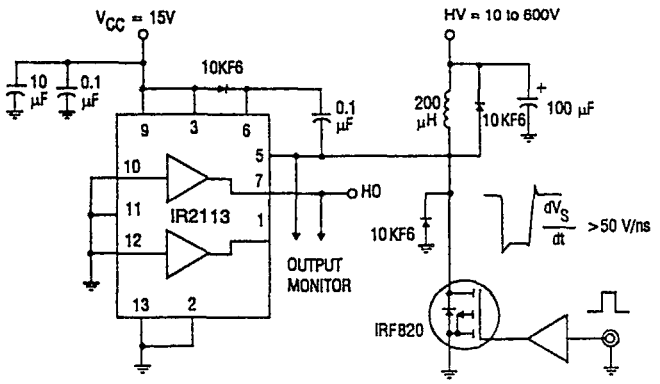


Figure 2. Floating Supply Voltage Transient Test Circuit

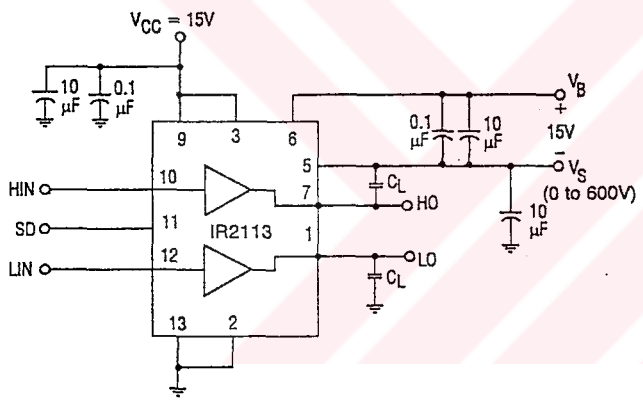


Figure 3. Switching Time Test Circuit

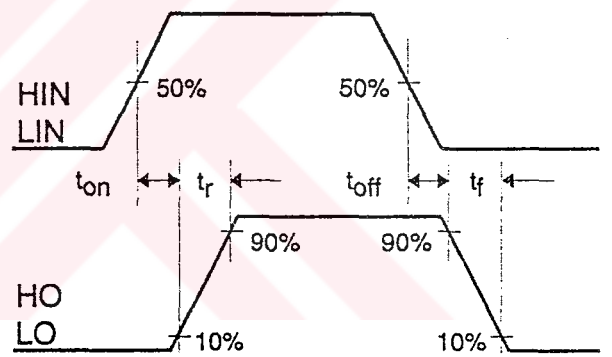


Figure 4. Switching Time Waveform Definition

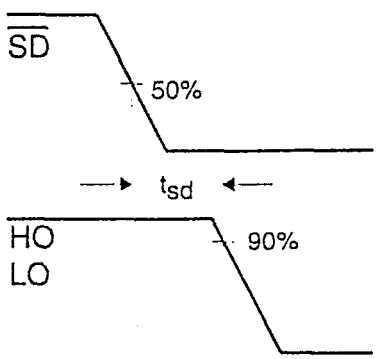


Figure 3. Shutdown Waveform Definitions

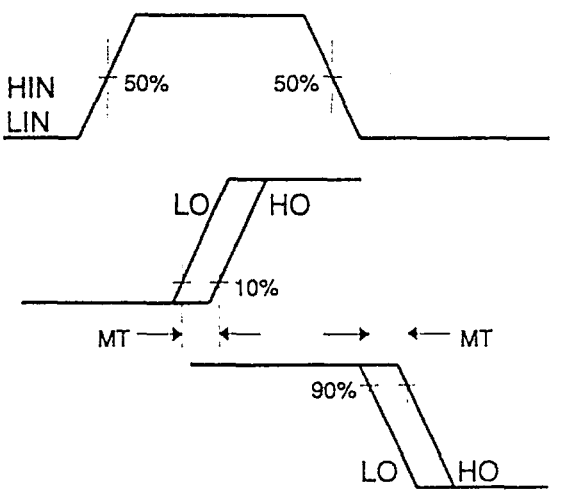


Figure 6. Delay Matching Waveform Definitions

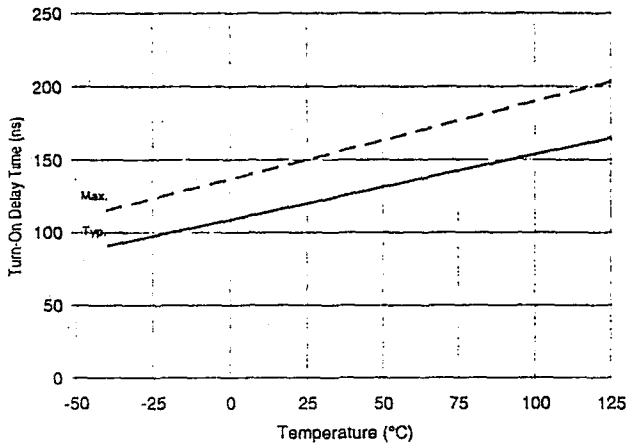


Figure 7A. Turn-On Time vs. Temperature

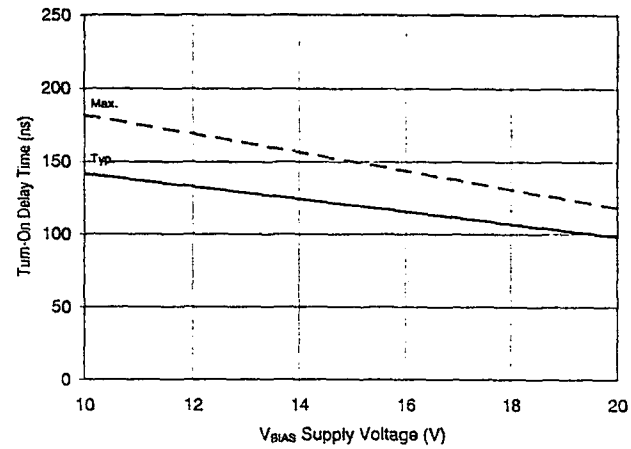


Figure 7B. Turn-On Time vs. Voltage

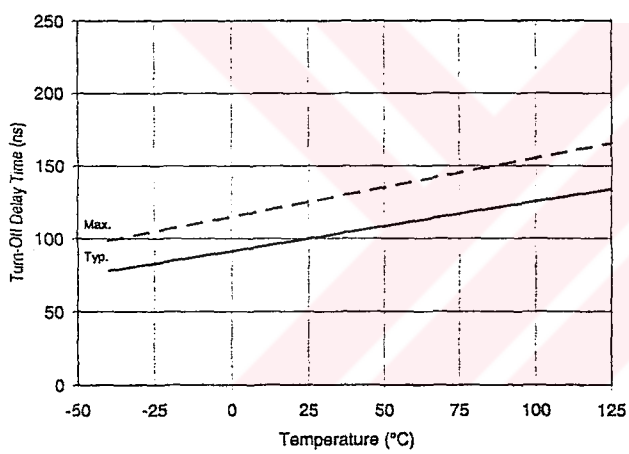


Figure 8A. Turn-Off Time vs. Temperature

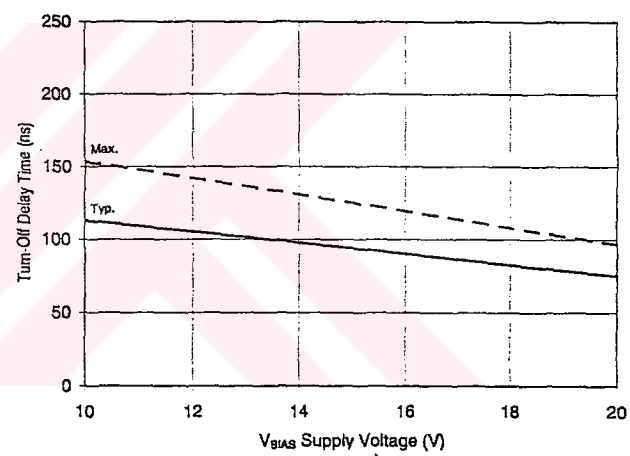


Figure 8B. Turn-Off Time vs. Voltage

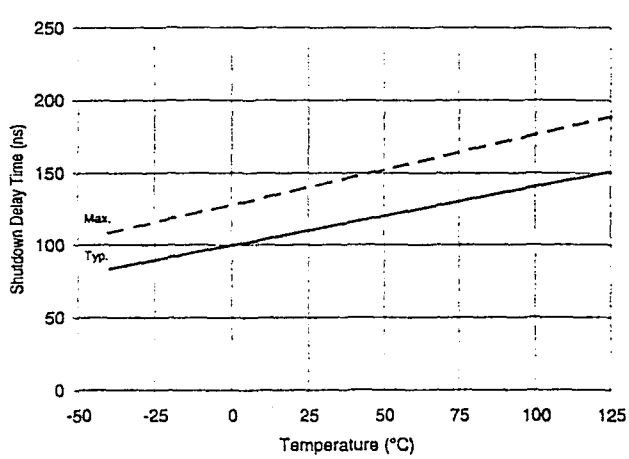


Figure 9A. Shutdown Time vs. Temperature

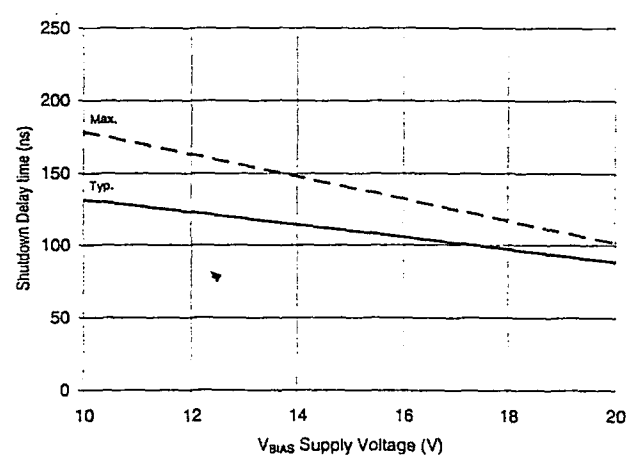


Figure 9B. Shutdown Time vs. Voltage

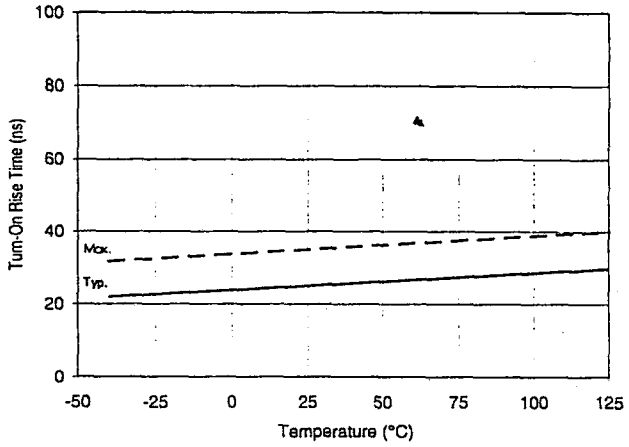


Figure 10A. Turn-On Rise Time vs. Temperature

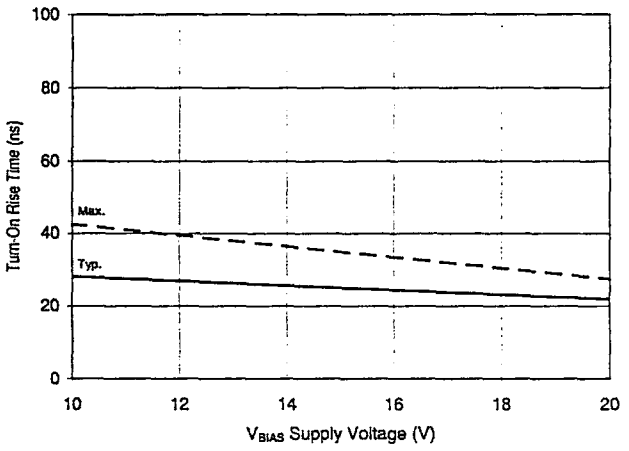


Figure 10B. Turn-On Rise Time vs. Voltage

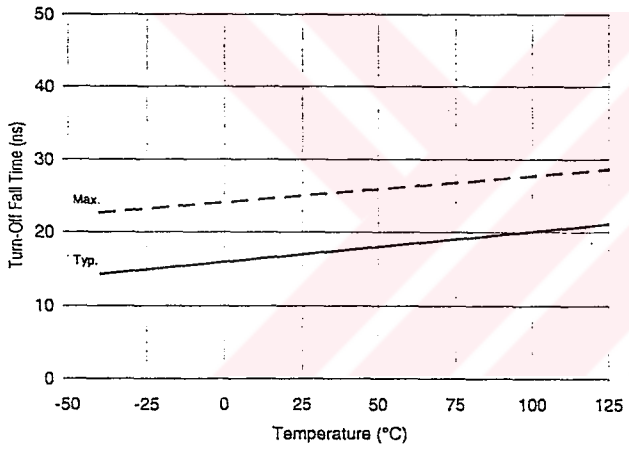


Figure 11A. Turn-Off Fall Time vs. Temperature

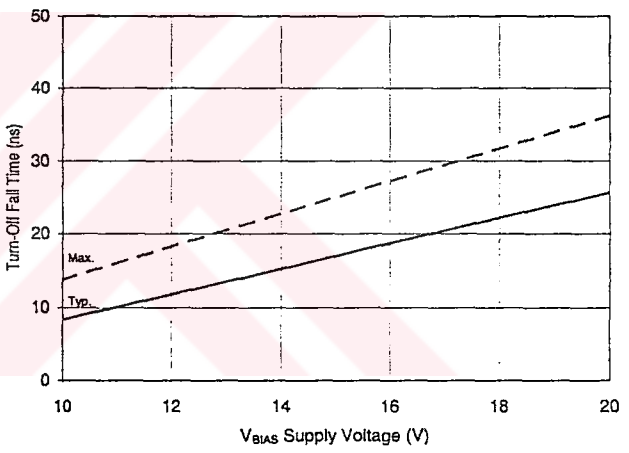


Figure 11B. Turn-Off Fall Time vs. Voltage

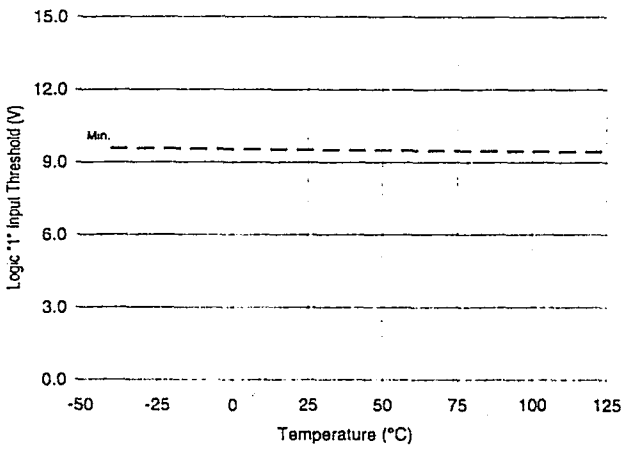


Figure 12A. Logic "1" Input Threshold vs. Temperature

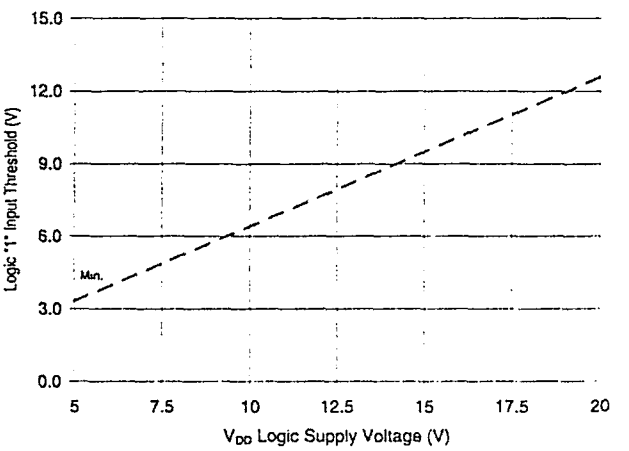


Figure 12B. Logic "1" Input Threshold vs. Voltage

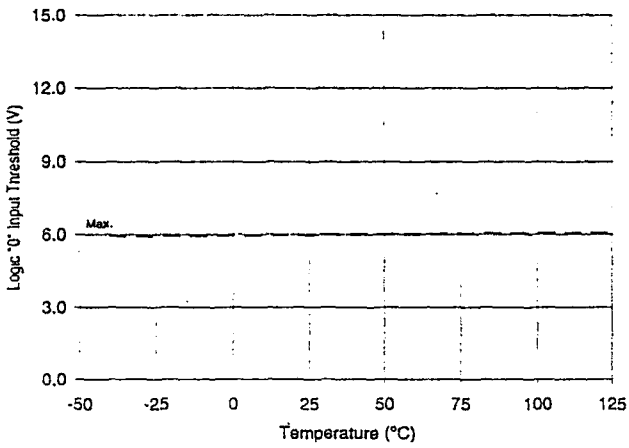


Figure 13A. Logic "0" Input Threshold vs. Temperature

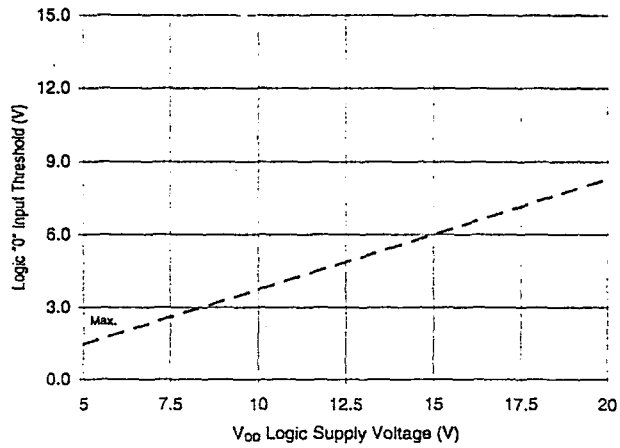


Figure 13B. Logic "0" Input Threshold vs. Voltage

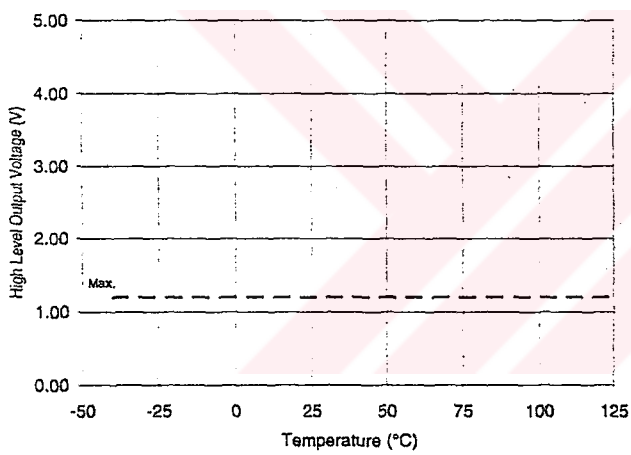


Figure 14A. High Level Output vs. Temperature

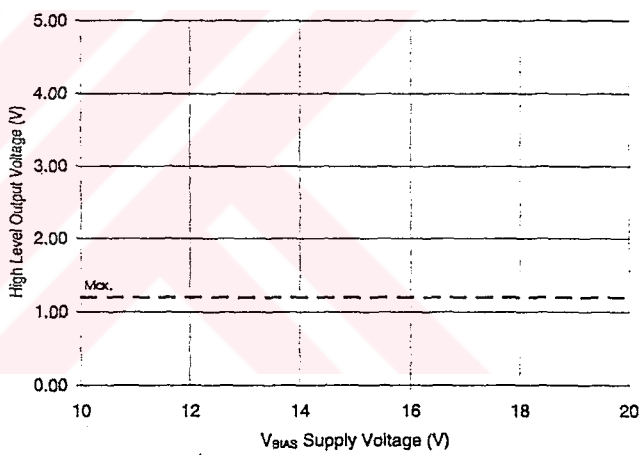


Figure 14B. High Level Output vs. Voltage

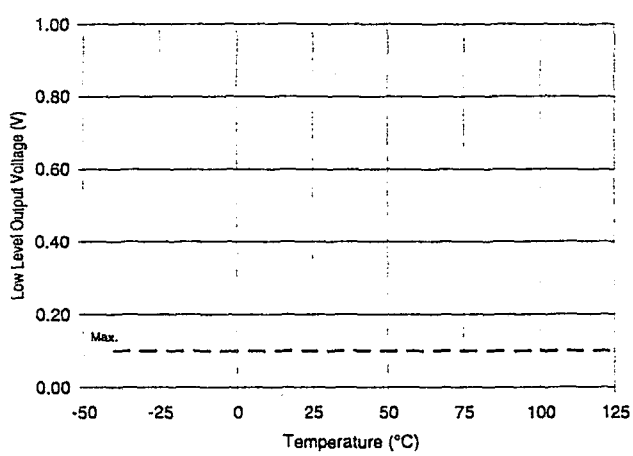


Figure 15A. Low Level Output vs. Temperature

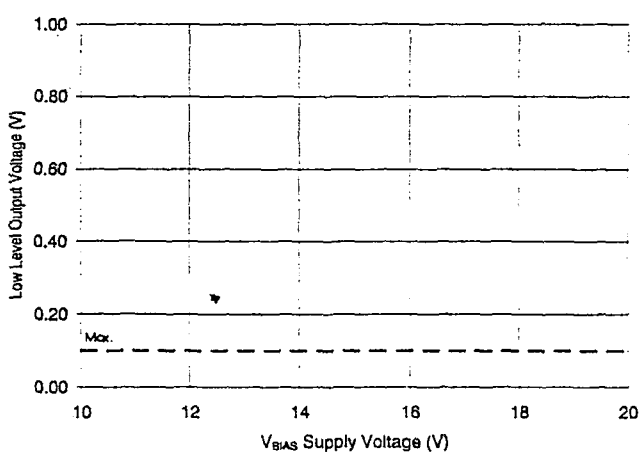


Figure 15B. Low Level Output vs. Voltage

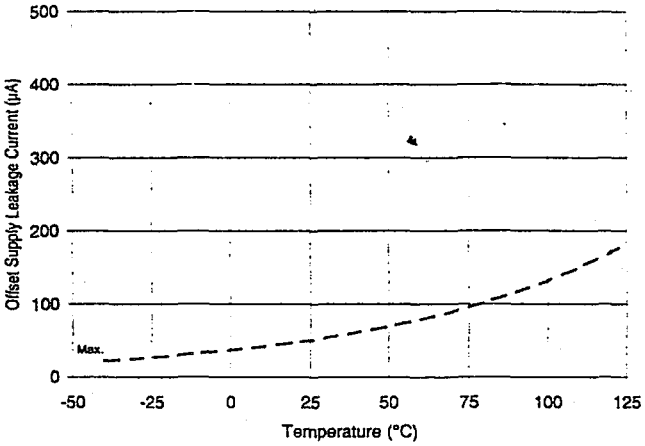


Figure 16A. Offset Supply Current vs. Temperature

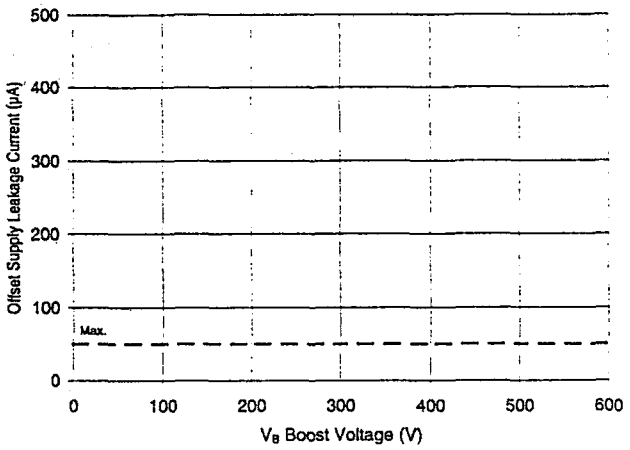


Figure 16B. Offset Supply Current vs. Voltage

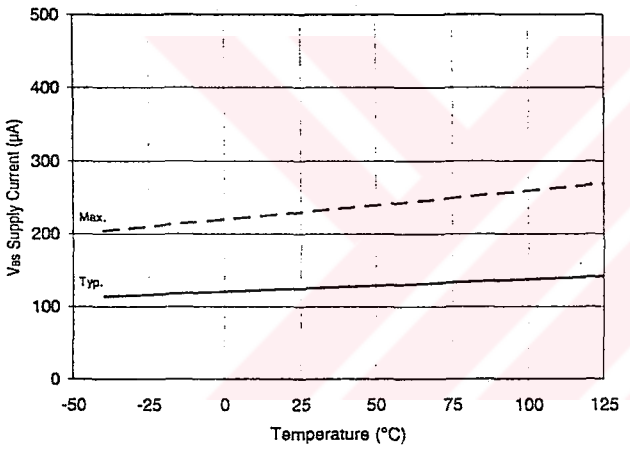


Figure 17A. V_{BS} Supply Current vs. Temperature

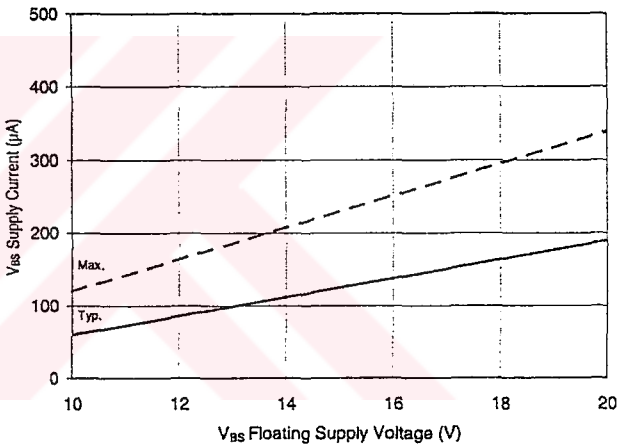


Figure 17B. V_{BS} Supply Current vs. Voltage

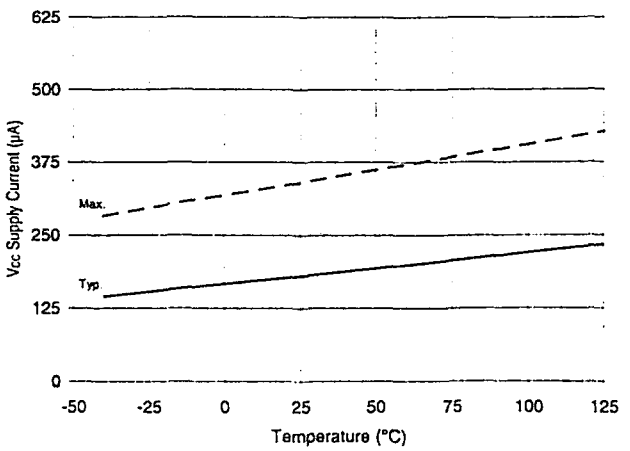


Figure 18A. V_{CC} Supply Current vs. Temperature

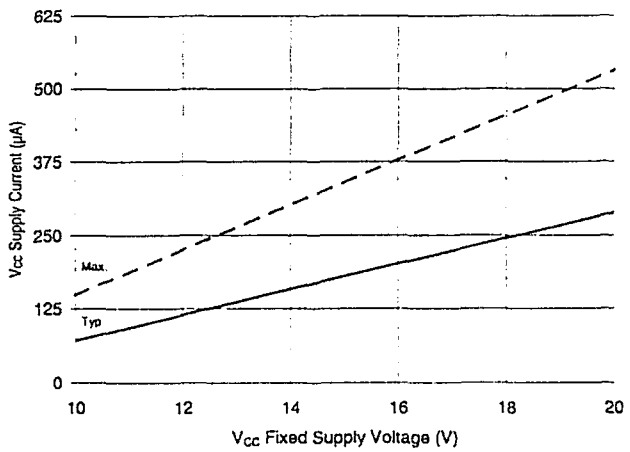


Figure 18B. V_{CC} Supply Current vs. Voltage

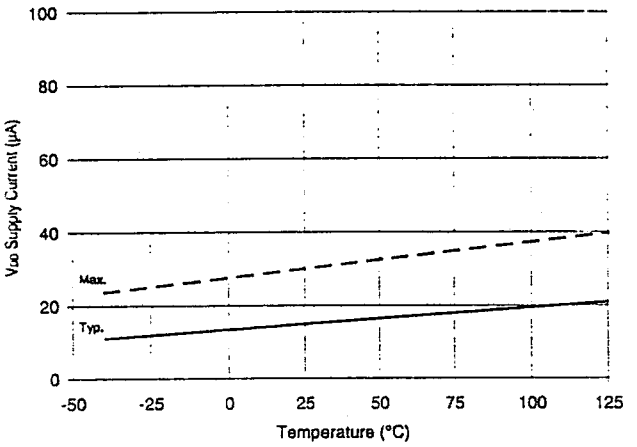


Figure 19A. V_{DD} Supply Current vs. Temperature

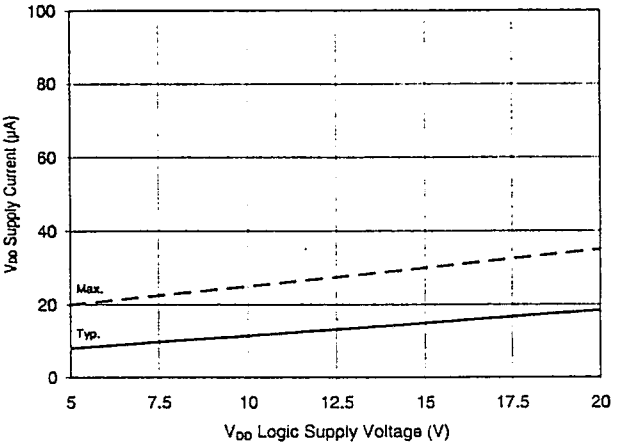


Figure 19B. V_{DD} Supply Current vs. Voltage

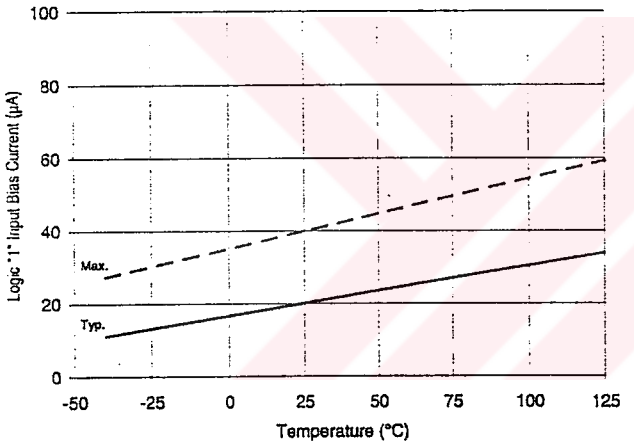


Figure 20A. Logic "1" Input Current vs. Temperature

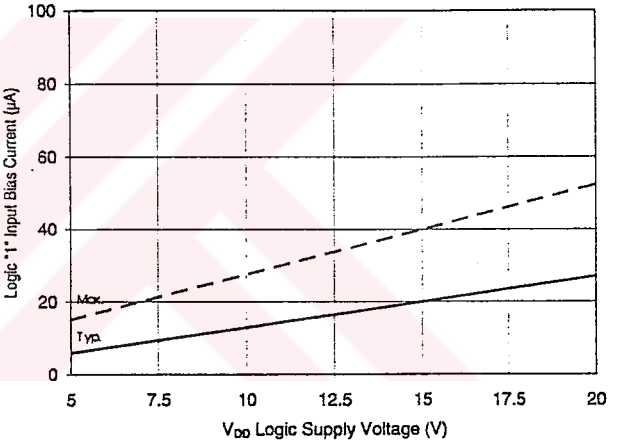


Figure 20B. Logic "1" Input Current vs. Voltage

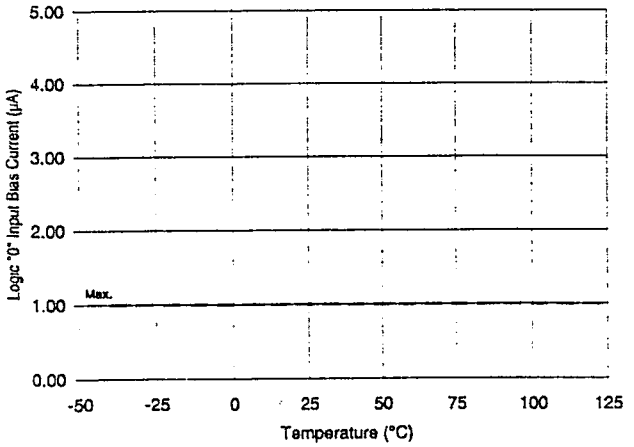


Figure 21A. Logic "0" Input Current vs. Temperature

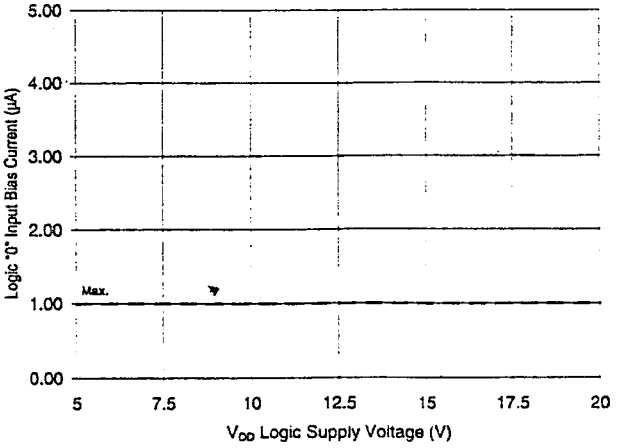


Figure 21B. Logic "0" Input Current vs. Voltage

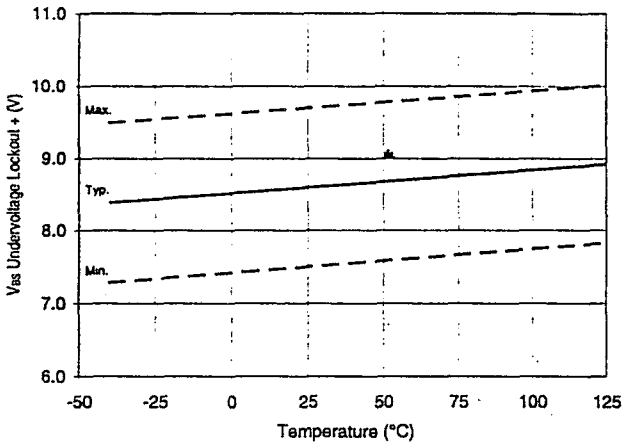


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

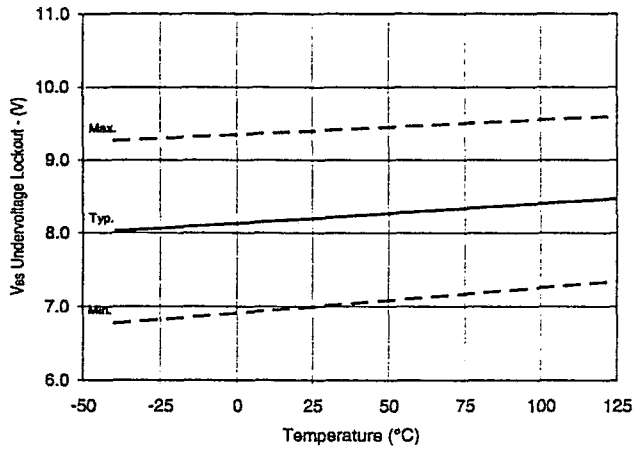


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

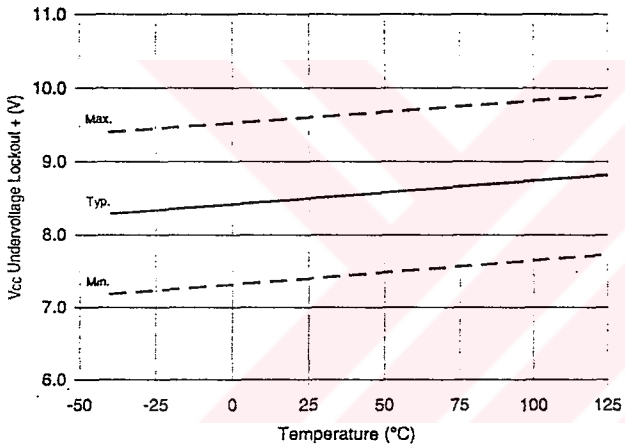


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

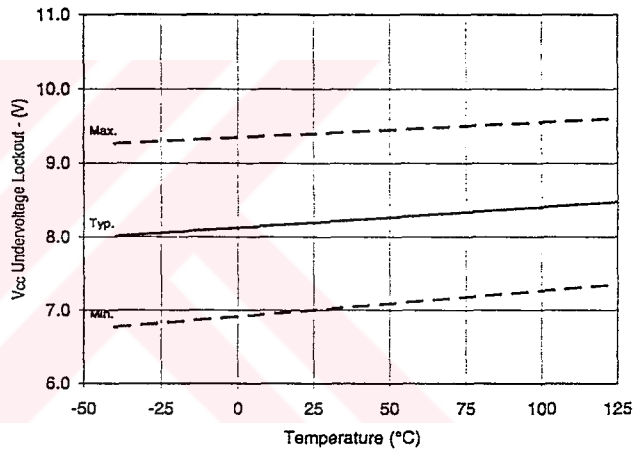


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

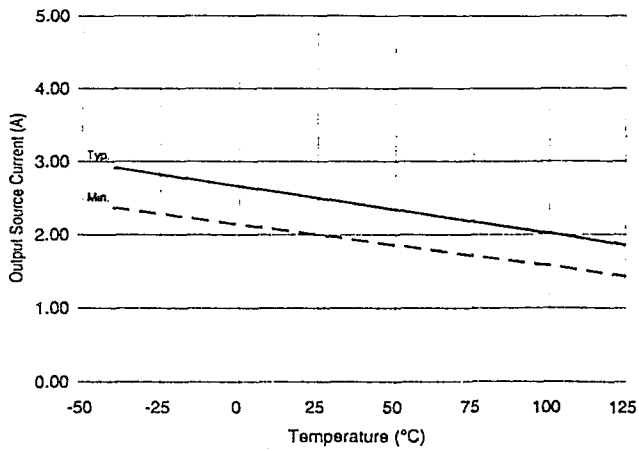


Figure 26A. Output Source Current vs. Temperature

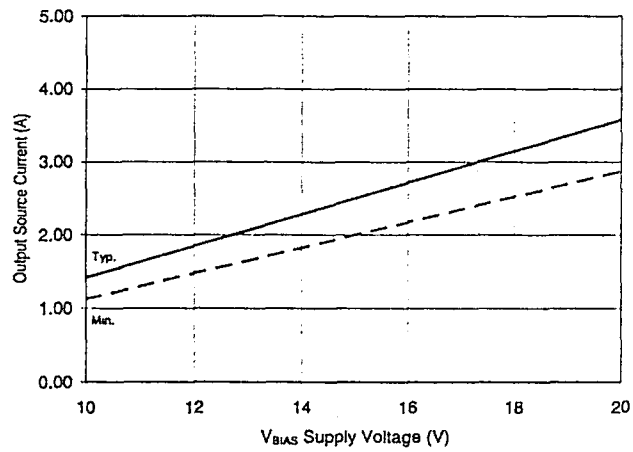


Figure 26B. Output Source Current vs. Voltage

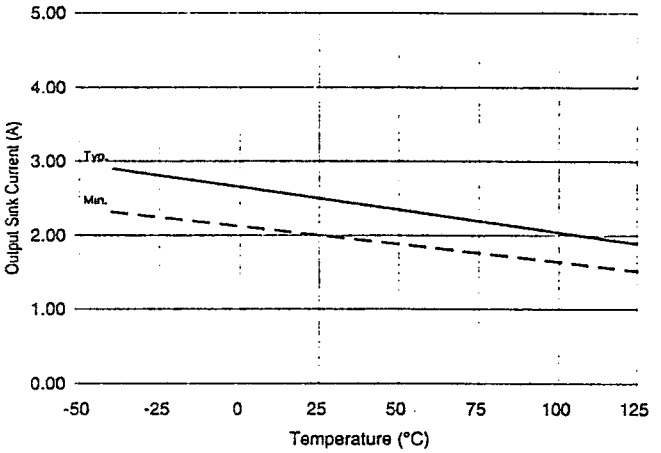


Figure 27A. Output Sink Current vs. Temperature

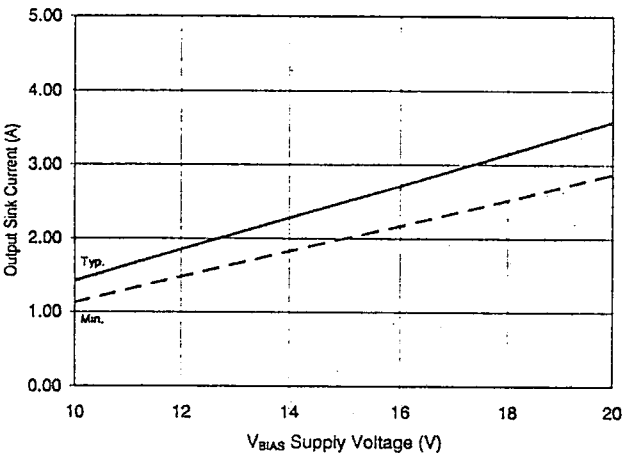


Figure 27B. Output Sink Current vs. Voltage

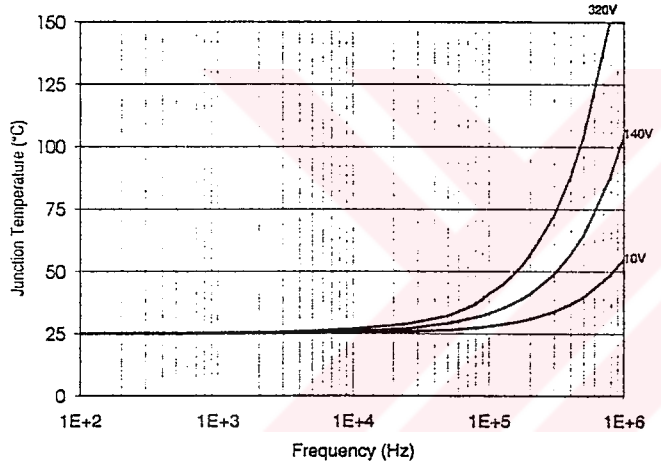


Figure 28. IR2113 T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

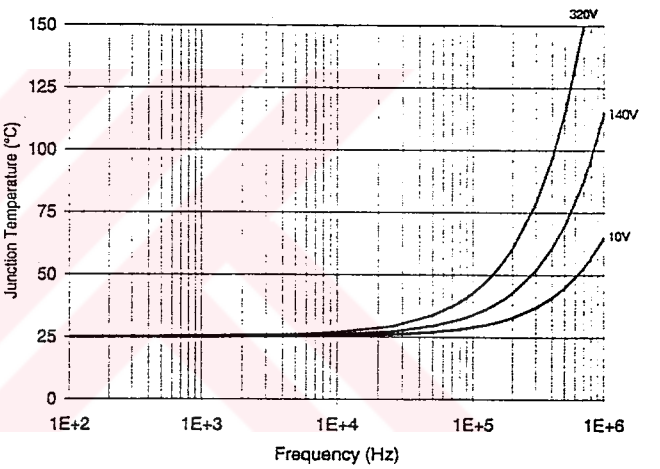


Figure 29. IR2113 T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

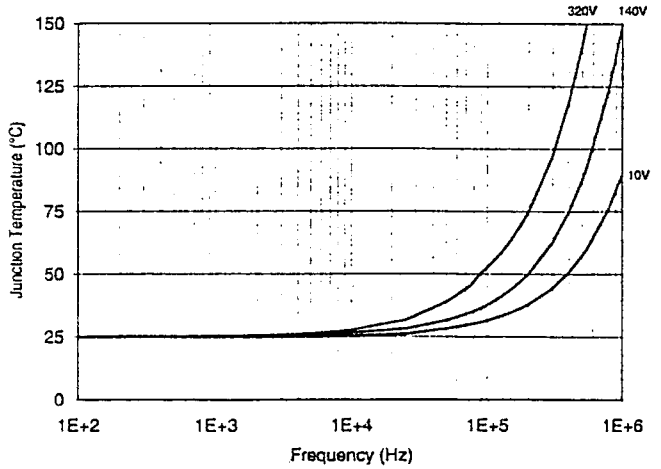


Figure 30. IR2113 T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

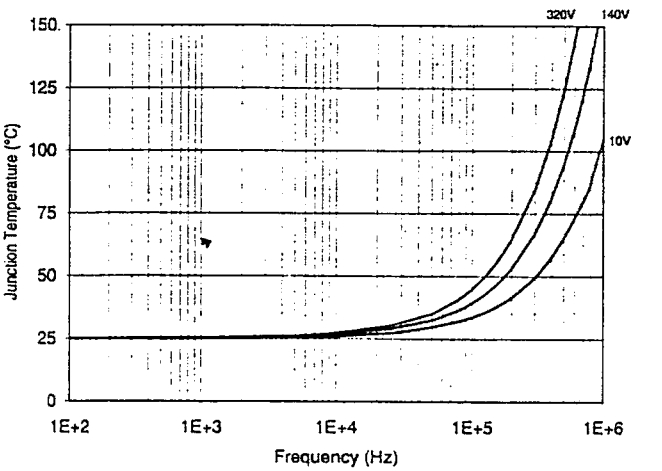


Figure 31. IR2113 T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

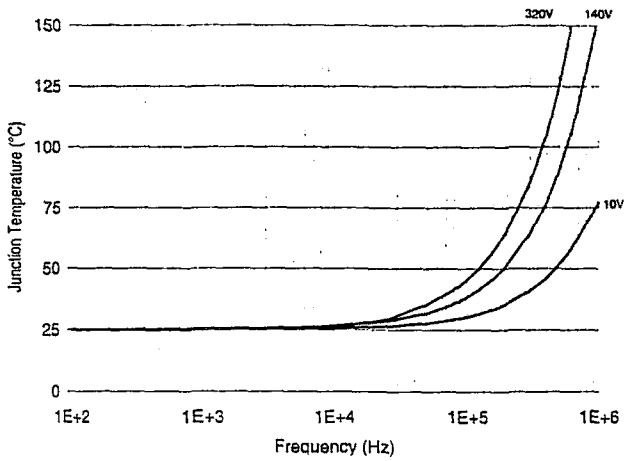


Figure 32. IR2113S T_J vs. Frequency (IRFBC20)
R_{GATE} = 33Ω, V_{CC} = 15V

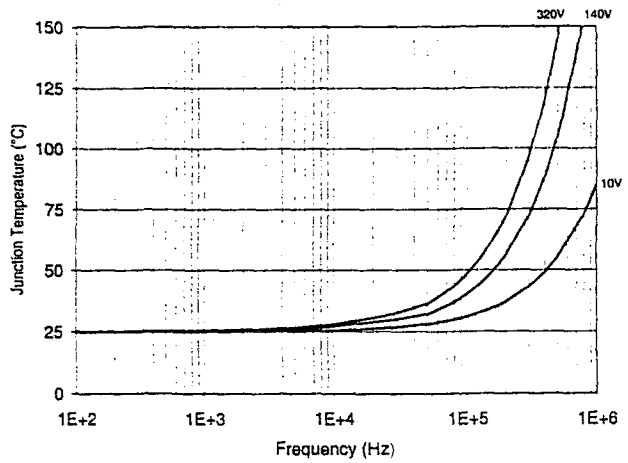


Figure 33. IR2113S T_J vs. Frequency (IRFBC30)
R_{GATE} = 22Ω, V_{CC} = 15V

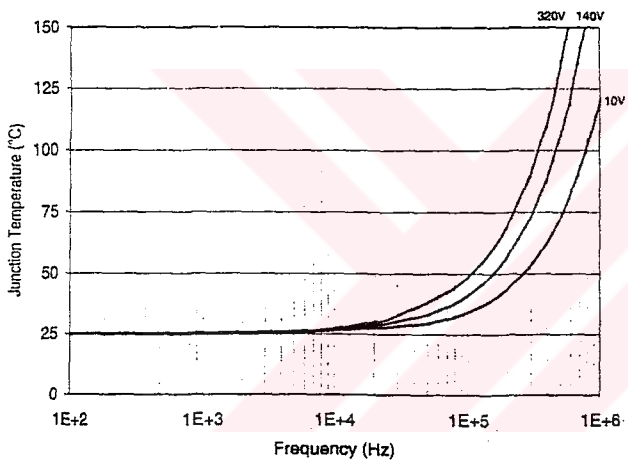


Figure 34. IR2113S T_J vs. Frequency (IRFBC40)
R_{GATE} = 15Ω, V_{CC} = 15V

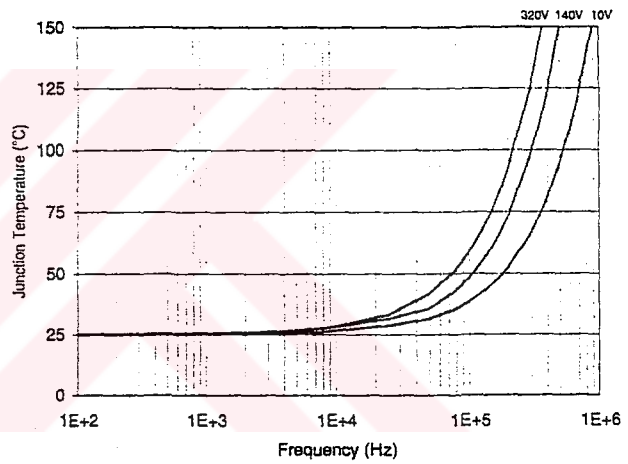


Figure 35. IR2113S T_J vs. Frequency (IRFPE50)
R_{GATE} = 10Ω, V_{CC} = 15V

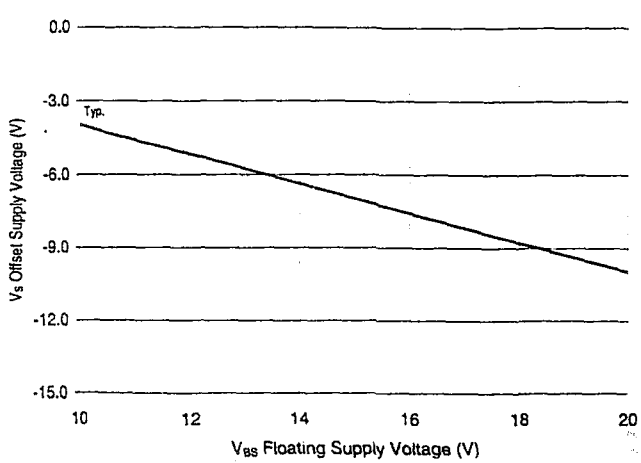


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

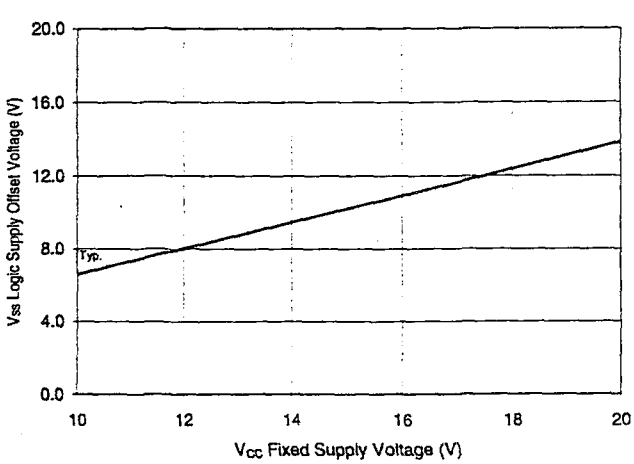


Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage